
EmETX-a55E0

AMD Fusion G-series ETX® CPU Module

User's Manual

Version 1.0



2012.06

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Chapter 1

Introduction

1.1 Copyright Notice

All Rights Reserved.

The information in this document is subject to change without prior notice in order to improve the reliability, design and function. It does not represent a commitment on the part of the manufacturer.

Under no circumstances will the manufacturer be liable for any direct, indirect, special, incidental, or consequential damages arising from the use or inability to use the product or documentation, even if advised of the possibility of such damages.

This document contains proprietary information protected by copyright. All rights are reserved. No part of this manual may be reproduced by any mechanical, electronic, or other means in any form without prior written permission of the manufacturer.

1.2 Declaration of Conformity

CE

The CE symbol on your product indicates that it is in compliance with the directives of the Union European (EU). A Certificate of Compliance is available by contacting Technical Support.

This product has passed the CE test for environmental specifications when shielded cables are used for external wiring. We recommend the use of shielded cables. This kind of cable is available from ARBOR. Please contact your local supplier for ordering information.

This product has passed the CE test for environmental specifications. Test conditions for passing included the equipment being operated within an industrial enclosure. In order to protect the product from being damaged by ESD (Electrostatic Discharge) and EMI leakage, we strongly recommend the use of CE-compliant industrial enclosure products.

Warning

This is a class A product. In a domestic environment this product may cause radio interference in which case the user may be required to take adequate measures.

FCC Class A

This device complies with Part 15 of the FCC Rules. Operation is subject to the following two conditions:

- (1) This device may not cause harmful interference, and
- (2) This device must accept any interference received, including interference that may cause undesired operation.

NOTE:

This equipment has been tested and found to comply with the limits for a Class A digital device, pursuant to Part 15 of the FCC Rules. These limits are designed to provide reasonable protection against harmful interference when the equipment is operated in a commercial environment. This equipment generates, uses, and can radiate radio frequency energy and, if not installed and used in accordance with the instruction manual, may cause harmful interference to radio communications. Operation of this equipment in a residential area is likely to cause harmful interference in which case the user will be required to correct the interference at his own expense.

RoHS

ARBOR Technology Corp. certifies that all components in its products are in compliance and conform to the European Union's Restriction of Use of Hazardous Substances in Electrical and Electronic Equipment (RoHS) Directive 2002/95/EC.

The above mentioned directive was published on 2/13/2003. The main purpose of the directive is to prohibit the use of lead, mercury, cadmium, hexavalent chromium, polybrominated biphenyls (PBB), and polybrominated diphenyl ethers (PBDE) in electrical and electronic products. Member states of the EU are to enforce by 7/1/2006.

ARBOR Technology Corp. hereby states that the listed products do not contain unintentional additions of lead, mercury, hex chrome, PBB or PBDB that exceed a maximum concentration value of 0.1% by weight or for cadmium exceed 0.01% by weight, per homogenous material. Homogenous material is defined as a substance or mixture of substances with uniform composition (such as solders, resins, plating, etc.). Lead-free solder is used for all terminations (Sn(96-96.5%), Ag(3.0-3.5%) and Cu(0.5%)).

SVHC / REACH

To minimize the environmental impact and take more responsibility to the earth we live, Arbor hereby confirms all products comply with the restriction of SVHC (Substances of Very High Concern) in (EC) 1907/2006 (REACH --Registration, Evaluation, Authorization, and Restriction of Chemicals) regulated by the European Union.

All substances listed in SVHC < 0.1 % by weight (1000 ppm)

1.3 About This User's Manual

This user's manual provides general information and installation instructions about the product. This User's Manual is intended for experienced users and integrators with hardware knowledge of personal computers. If you are not sure about any description in this booklet, please consult your vendor before further handling.

1.4 Warning

Single Board Computers and their components contain very delicate Integrated Circuits (IC). To protect the Single Board Computer and its components against damage from static electricity, you should always follow the following precautions when handling it :

1. Disconnect your Single Board Computer from the power source when you want to work on the inside.
2. Hold the board by the edges and try not to touch the IC chips, leads or circuitry.
3. Use a grounded wrist strap when handling computer components.
4. Place components on a grounded antistatic pad or on the bag that comes with the Single Board Computer, whenever components are separated from the system.

1.5 Replacing the Lithium Battery

Incorrect replacement of the lithium battery may lead to a risk of explosion.

The lithium battery must be replaced with an identical battery or a battery type recommended by the manufacturer.

Do not throw lithium batteries into the trash-can. It must be disposed of in accordance with local regulations concerning special waste.

1.6 Technical Support

If you have any technical difficulties, please do not hesitate to call or e-mail our customer service.

<http://www.arbor.com.tw>

E-mail:info@arbor.com.tw

1.7 Warranty

This product is warranted to be in good working order for a period of two years from the date of purchase. Should this product fail to be in good working order at any time during this period, we will, at our option, replace or repair it at no additional charge except as set forth in the following terms. This warranty does not apply to products damaged by misuse, modifications, accident or disaster.

Vendor assumes no liability for any damages, lost profits, lost savings or any other incidental or consequential damage resulting from the use, misuse of, or inability to use this product. Vendor will not be liable for any claim made by any other related party.

Vendors disclaim all other warranties, either expressed or implied, including but not limited to implied warranties of merchantability and fitness for a particular purpose, with respect to the hardware, the accompanying product's manual(s) and written materials, and any accompanying hardware. This limited warranty gives you specific legal rights.

Return authorization must be obtained from the vendor before returned merchandise will be accepted. Authorization can be obtained by calling or faxing the vendor and requesting a Return Merchandise Authorization (RMA) number. Returned goods should always be accompanied by a clear problem description.

1.8 Packing List

Before you begin installing your single board, please make sure that the following materials have been shipped:



1 x EmETX-a55E0 ETX® CPU Module



1 x Driver CD



1 x Quick Installation Guide

If any of the above items is damaged or missing, contact your vendor immediately.

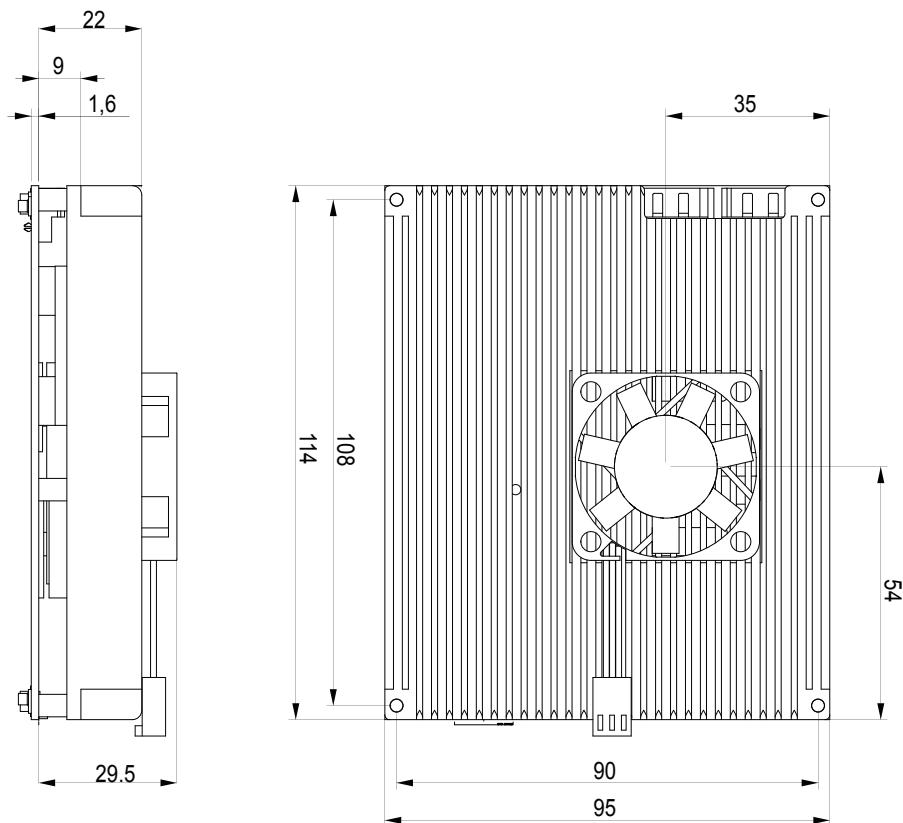
1.9 Ordering Information

EmETX-a55E0-T56N	AMD G-T56N Dual Core ETX CPU Module
HS-55E0-F1	Heat spreader
HS-55E0-C1	CPU module cooler for 18W APU (114*95*29.5mm)
PBE-1000 R2.1	ETX® evaluation board in ATX form factor
CBK-05-1000-00	Cable kit 3 x COM port cables 1 x USB cable 2 x IDE cables

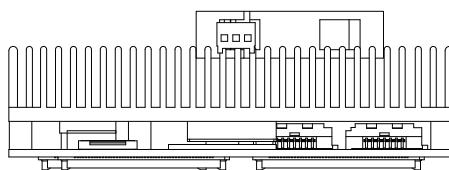
1.10 Specifications

Form Factor	ETX® CPU Module
CPU	Soldered onboard AMD G-Fusion T-56N 1.65GHz Processor
Chipset	AMD FCH A55E
System Memory	1 x 204-pin DDR3 SO-DIMM Socket up to 4GB 1333MHz SDRAM
VGA/ LCD Controller	Integrated Radeon HD 6320 with Analog RGB/ 24-bit dual channels LVDS (Dual independent displays)
Ethernet	1 x Realtek RTL8105EL 10/100 Base-T Ethernet
Audio	Realtek ALC886 7.1 Channel HD Audio Codec, support Mic-in/Line-in/Line-out
BIOS	AMI PnP Flash UEFI BIOS
Serial ATA	2 x Serial ATA with 300MB/s HDD transfer rate
IDE Interface	2 x Ultra ATA, support 4 IDE devices
Serial Port	2 x COM Ports (1 x RS-232, 1 x RS-232/422/485 selectable via PBE-1000)
Parallel Port	1 x SPP/EPP/ECP mode
KB/MS	Support PS/2 interface Keyboard and Mouse
Universal Serial Bus	4 x USB 2.0 ports
LCD	Dual Channels 24-bit LVDS
DDI output	Supports extra DisplayPort connector
Expansion Interface	4 x PCI masters and ISA Bus LPC interface DDI port connector on CPU module
Operation Temp.	-20°C ~ 70°C (-4°F~158°F)
Watchdog Timer	1~255 level Reset
Dimension (L x W)	114 x 95 mm (4.5" x 3.7")

1.11 Board Dimensions



Unit: mm





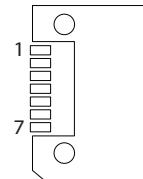
Chapter 2

Installation

2.1 Connectors

SATA1, SATA2 Connectors

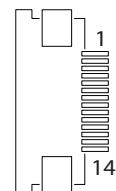
Pin	Description
1	GND
2	TX+
3	TX-
4	GND
5	RX-
6	RX+
7	GND



LPC1 Connector

Connector type: FPC12-14P-P0.5 (Hirose)

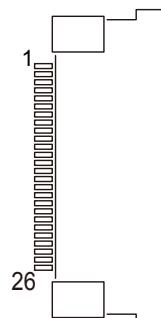
Pin	Description	Pin	Description
1	LAD0	8	BUF_PLT_RST#
2	LAD1	9	GND
3	LAD2	10	PCLK_CONN
4	LAD3	11	GND
5	GND	12	GND
6	LFRAFME#	13	+3.3V
7	INT_SERIRQ	14	+3.3V



DDI1 Connector

Connector type: FH12-26S-0.5SH (Hirose)

Pin	Description	Pin	Description
1	GND	14	N/C
2	DDI_TX0+	15	DDI_AUX+
3	DDI_TX0-	16	DDI_AUX-
4	GND	17	GND
5	DDI_TX1+	18	DDI_HPD
6	DDI_TX1-	19	SMB_DAT
7	GND	20	SMB_CLK
8	DDI_TX2+	21	GND
9	DDI_TX2-	22	GND
10	GND	23	GND
11	DDI_TX3+	24	+3.3V
12	DDI_TX3-	25	+3.3V
13	GND	26	+5V



ETX1 Connector

A1	GND	GND	A2
A3	PC/CLK3	PC/CLK4	A4
A5	GND	GND	A6
A7	PC/CLK1	PC/CLK2	A8
A9	REQ#3	GNT#3	A10
A11	GNT#2	VCC3	A12
A13	REQ#2	GNT#1	A14
A15	REQ#1	VCC3	A16
A17	GNT#0	N.C	A18
A19	VCC	VCC	A20
A21	SERIRQ	REQ#0	A22
A23	AD0	VCC3	A24
A25	AD1	AD2	A26
A27	AD4	AD3	A28
A29	AD6	AD5	A30
A31	CBE#0	AD7	A32
A33	AD8	AD9	A34
A35	GND	GND	A36
A37	AD10	AUXAL	A38
A39	AD11	MIC	A40
A41	AD12	AUXAR	A42
A43	AD13	ASVCC	A44
A45	AD14	SNDL	A46
A47	AD15	ASGND	A48
A49	CBE#1	SNDR	A50
A51	VCC	VCC	A52
A53	PAR	SERR#	A54
A55	PERR#	N.C	A56
A57	PME#	USB2-	A58
A59	LOCK#	DEVSEL#	A60
A61	TRDY#	USB3-	A62
A63	IRDY#	STOP#	A64
A65	FRAME#	USB2+	A66
A67	GND	GND	A68
A69	AD16	CBE#2	A70
A71	AD17	USB3+	A72
A73	AD19	AD18	A74
A75	AD20	USB0-	A76
A77	AD22	AD21	A78
A79	AD23	USB1-	A80
A81	AD24	CBE#3	A82
A83	VCC	VCC	A84
A85	AD25	AD26	A86
A87	AD28	USB0+	A88
A89	AD27	AD29	A90
A91	AD30	USB1+	A92
A93	PCIRST#	AD31	A94
A95	INTR#C	INTR#D	A96
A97	INTR#A	INTR#B	A98
A99	GND	GND	A100

ETX2 Connector

B1	GND	GND	B2
B3	SD14	SD15	B4
B5	SD13	MASTER#	B6
B7	SD12	DREQ7	B8
B9	SD11	DACK7	B10
B11	SD10	DREQ6	B12
B13	SD9	DACK6	B14
B15	SD8	DREQ5	B16
B17	MEMW#	DACK5	B18
B19	MEMR#	DREQ0	B20
B21	LA17	DACK5#	B22
B23	LA18	IRQ14	B24
B25	LA19	IRQ15	B26
B27	LA20	IRQ12	B28
B29	LA21	IRQ11	B30
B31	LA22	IRQ10	B32
B33	LA23	IO16#	B34
B35	GND	GND	B36
B37	SBHE#	M16#	B38
B39	SA0	OSC	B40
B41	SA1	BALE	B42
B43	SA2	TC	B44
B45	SA3	DACK#2	B46
B47	SA4	IRQ3	B48
B49	SA5	IRQ4	B50
B51	VCC	VCC	B52
B53	SA6	IRQ5	B54
B55	SA7	IRQ6	B56
B57	SA8	IRQ7	B58
B59	SA9	SYSCLK	B60
B61	SA10	REFCH#	B62
B63	SA11	DREQ1	B64
B65	SA12	DACK#1	B66
B67	GND	GND	B68
B69	SA13	DREQ3	B70
B71	SA14	DACK#3	B72
B73	SA15	IOR#	B74
B75	SA16	IOW#	B76
B77	SA18	SA17	B78
B79	SA19	SMEMR#	B80
B81	IOCHRDY	AEN	B82
B83	VCC	VCC	B84
B85	SD0	SMEMW#	B86
B87	SD2	SD1	B88
B89	SD3	NOWS#	B90
B91	DREQ2	SD4	B92
B93	SD5	IRQ9	B94
B95	SD9	SD7	B96
B97	IOCHK#	RSTDVR	B98
B99	GND	GND	B100

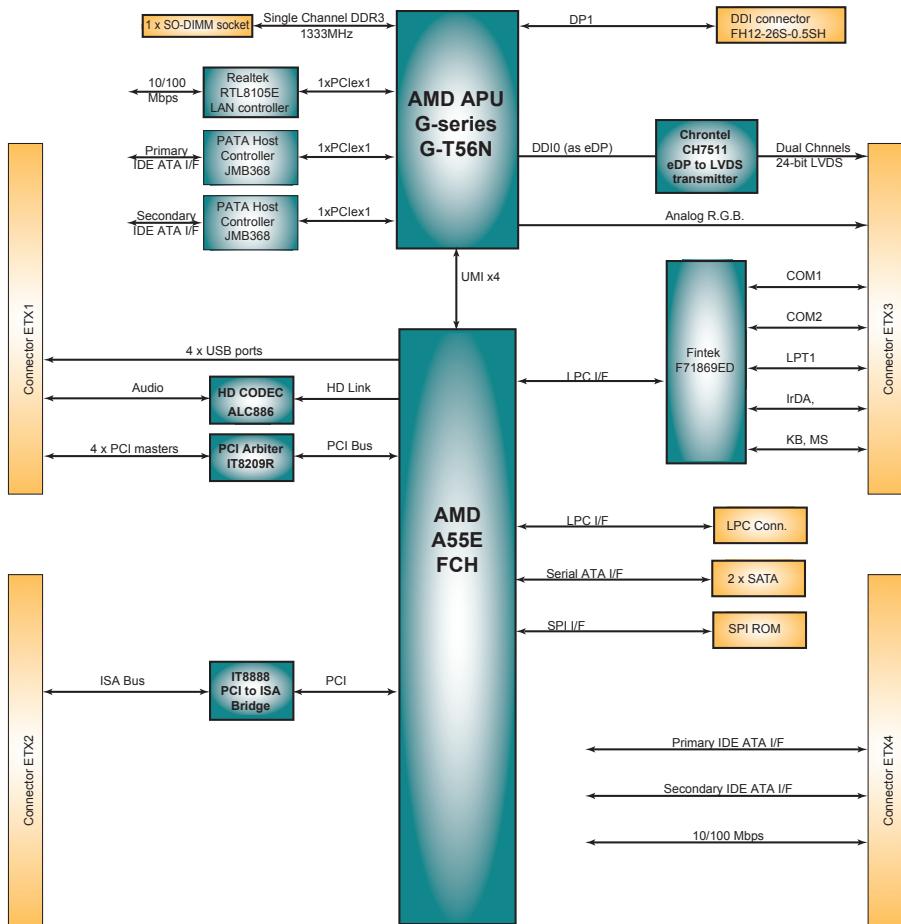
ETX3 Connector

C1	GND	GND	C2
C3	R	B	C4
C5	HSY	G	C6
C7	VSY	Analog RGB_DDC_CLK	C8
C9	DETECT#	Analog RGB_DDC_ATA	C10
C11	TX2CLK#	N.C.	C12
C13	TX2CLK	N.C.	C14
C15	GND	GND	C16
C17	TX2D1	TX2D2	C18
C19	TX2D1#	TX2D2#	C20
C21	GND	GND	C22
C23	N.C.	TX2D0	C24
C25	N.C.	TX2D0#	C26
C27	GND	GND	C28
C29	TX1D2#	TX1CLK	C30
C31	TX1D2	TX1CLK#	C32
C33	GND	GND	C34
C35	TX1D0	TX1D1	C36
C37	TX1D0#	TX1D1#	C38
C39	VCC	VCC	C40
C41	DDC_DATA	N.C.	C42
C43	DDC_CLK	BLON#	C44
C45	BKLTCCTL	VDDEN	C46
C47	TV_DATA_COMP	Y	C48
C49	N.C.	C	C50
C51	LPT/FLPY#	N.C.	C52
C53	VCC	GND	C54
C55	STB#	AFD#/DENSEL	C56
C57	N.C.	PD7/N.C	C58
C59	IRRX	ERR#/HDSEL#	C60
C61	IRTX	PD6/N.C	C62
C63	RXD2	INIT#/DIR#	C64
C65	GND	GND	C66
C67	RTS#2	PD5/N.C	C68
C69	DTR#2	SLIN#/STEP#	C70
C71	DCD#2	PD4/DSKCHG#	C72
C73	DSR#2	PD3/RDATA#	C74
C75	CTS#2	PD2/WP#	C76
C77	TXD#2	PD1/TRK0#	C78
C79	R#2	PD0/INDEX#	C80
C81	VCC	VCC	C82
C83	RXD1	ACK#/DRV	C84
C85	RTS#1	BUSY#/MOT	C86
C87	DTR#1	PE/MDATA#	C88
C89	DCD#1	SLCT#/WGATE#	C90
C91	DSR#1	MSCLK	C92
C93	CTS#1	MSDAT	C94
C95	TXD#1	KBCLK	C96
C97	R#1	KBDAT	C98
C99	GND	GND	C100

ETX4 Connector

D1	GND	GND	D2
D3	5V_SB	PWGIN	D4
D5	PS_ON	SPEAKER	D6
D7	PWERBTN#	BATT	D8
D9	KBINH	LILED	D10
D11	RSMRST#	ACTLED	D12
D13	N.C	SPEEDLED	D14
D15	N.C	I2CLK	D16
D17	VCC	VCC	D18
D19	OVCR#	N.C	D20
D21	EXTSMI#	I2DAT	D22
D23	SMBCLK	SMBDAT	D24
D25	SIDE_CS1#	SMBALRT#	D26
D27	SIDE_CS0#	SATALED#	D28
D29	SIDE_A2	PIDE_CS3#	D30
D31	SIDE_A0	PIDE_CS1#	D32
D33	GND	GND	D34
D35	PDIAG_S	PIDE_A2	D36
D37	SIDE_A1	PIDE_A0	D38
D39	SIDE_INTRQ	PIDE_A1	D40
D41	BATLOW#	N.C	D42
D43	SIDE_ACK#	PIDE_INTRQ	D44
D45	SIDE_RDY	PIDE_ACK#	D46
D47	SIDE_IOR#	PIDE_RDY	D48
D49	VCC	VCC	D50
D51	SIDE_IOW#	PIDE_IOR#	D52
D53	SIDE_DRQ	PIDE_IOW#	D54
D55	SIDE_D15	PIDE_DRQ	D56
D57	SIDE_D0	PIDE_D15	D58
D59	SIDE_D14	PIDE_D0	D60
D61	SIDE_D1	PIDE_D14	D62
D63	SIDE_D13	PIDE_D1	D64
D65	GND	GND	D66
D67	SIDE_D2	PIDE_D13	D68
D69	SIDE_D12	PIDE_D2	D70
D71	SIDE_D3	PIDE_D12	D72
D73	SIDE_D11	PIDE_D3	D74
D75	SIDE_D4	PIDE_D11	D76
D77	SIDE_D10	PIDE_D4	D78
D79	SIDE_D5	PIDE_D10	D80
D81	VCC	VCC	D82
D83	SIDE_D9	PIDE_D5	D84
D85	SIDE_D6	PIDE_D9	D86
D87	SIDE_D8	PIDE_D6	D88
D89	GPE2#	CBLID_P#	D90
D91	RXD-	PIDE_D8	D92
D93	RXD+	N.C	D94
D95	TXD-	PIDE_D7	D96
D97	TXD+	HDRST#	D98
D99	GND	GND	D100

2.2 Block Diagram



2.3 Driver Installation Paths

Windows 2000 & XP

Driver	Path
CHIPSET & VGA	\EmETX-a55E0\GRAPHICS\XP\8.92-111109a-129010C-EDG_Direct
LAN	\EmETX-a55E0\ETHERNET\WinXP\PCIE_Install_5792_01142012
AUDIO	\EmETX-a55E0\AUDIO\WinXP\WDM_R267

Windows 7

Driver	Path
CHIPSET & VGA	\EmETX-a55E0\GRAPHICS\Win7\8.92-111109a-129011C-EDG_Direct
LAN	\EmETX-a55E0\ETHERNET\win7\Install_Win7_7050_01162012
AUDIO	\EmETX-a55E0\AUDIO\Win7\Vista_Win7_R267

Chapter 3

BIOS

3.1 BIOS Main Setup

The AMI BIOS provides a setup utility program for specifying the system configurations and settings which are stored in the BIOS ROM of the system. When you turn on the computer, the AMI BIOS is immediately activated. After you have entered the setup utility, use the left/right arrow keys to highlight a particular configuration screen from the top menu bar or use the down arrow key to access and configure the information below.

NOTE: In order to increase system stability and performance, our engineering staff are constantly improving the BIOS menu. The BIOS setup screens and descriptions illustrated in this manual are for your reference only, and may not completely match what you see on your screen.



BIOS Information

Display the BIOS information.

System Date

Set the system date. Note that the 'Day' automatically changes when you set the date.

The date format is:

Day : Sun to Sat
Month : 1 to 12
Date : 1 to 31
Year : 1998 to 2099

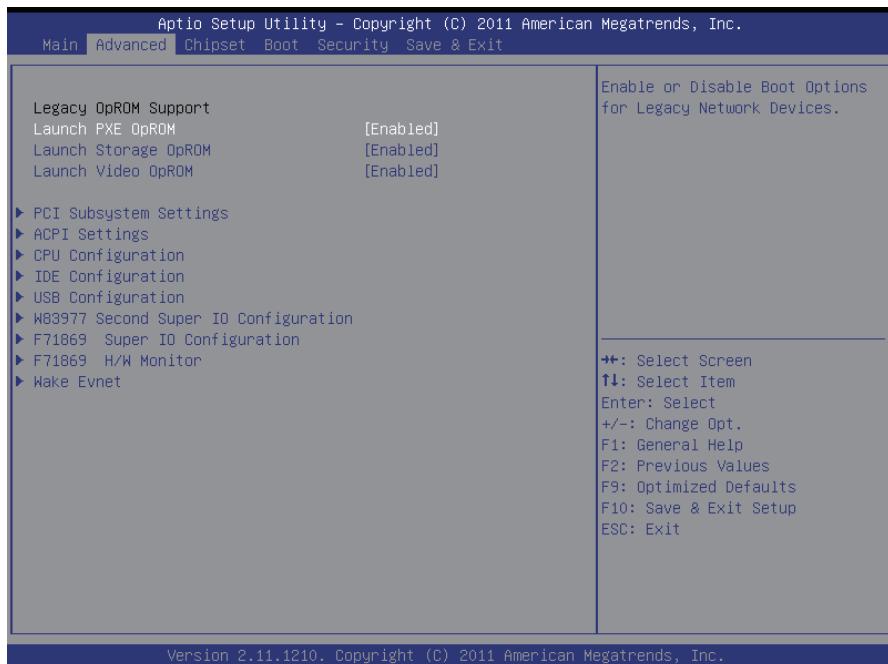
System Time

Set the system time.

The time format is:

Hour : 00 to 23
Minute : 00 to 59
Second : 00 to 59

3.2 Advanced Settings



Legacy OpROM Support

Launch PXE OpROM

Enable or disable the boot option for legacy network devices.

Launch Storage OpROM

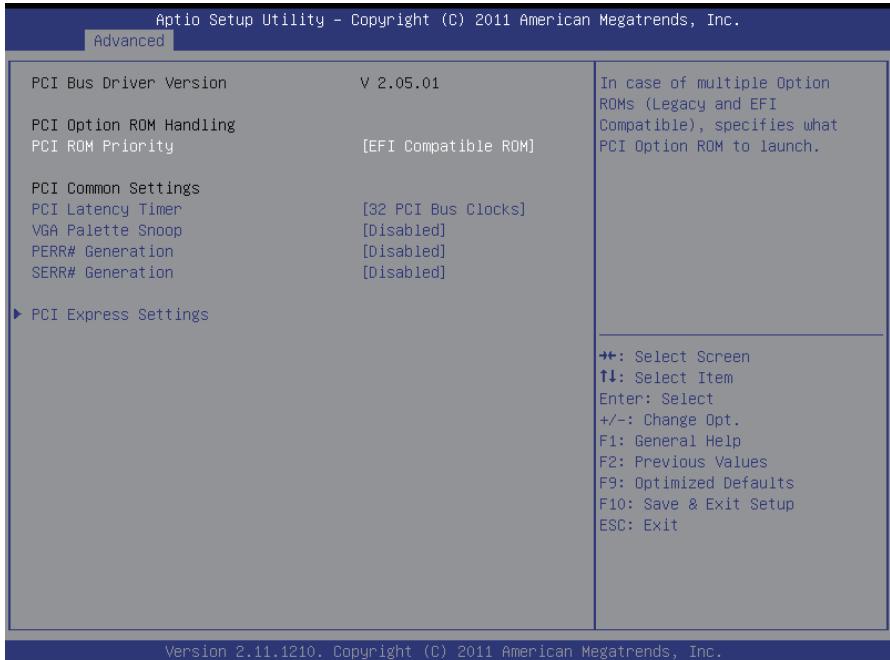
Enable or Disable Boot Option for Legacy Mass Storage Devices with Option ROM.

Launch Video OpROM

Execution of the Legacy Option ROM for video devices.

The choice: Enabled (Default), Disabled, Enabled when no UEFI driver

3.2.1 PCI Subsystem Settings



PCI ROM Priority

In case of multiple Option ROMs (Legacy and EFI Compatible), specifies what PCI Option ROM to launch.

PCI Latency Timer

Value to be programmed into PCI Latency Timer Register.

VGA Palette Snoop

Enables or Disables VGA Palette Registers Snooping.

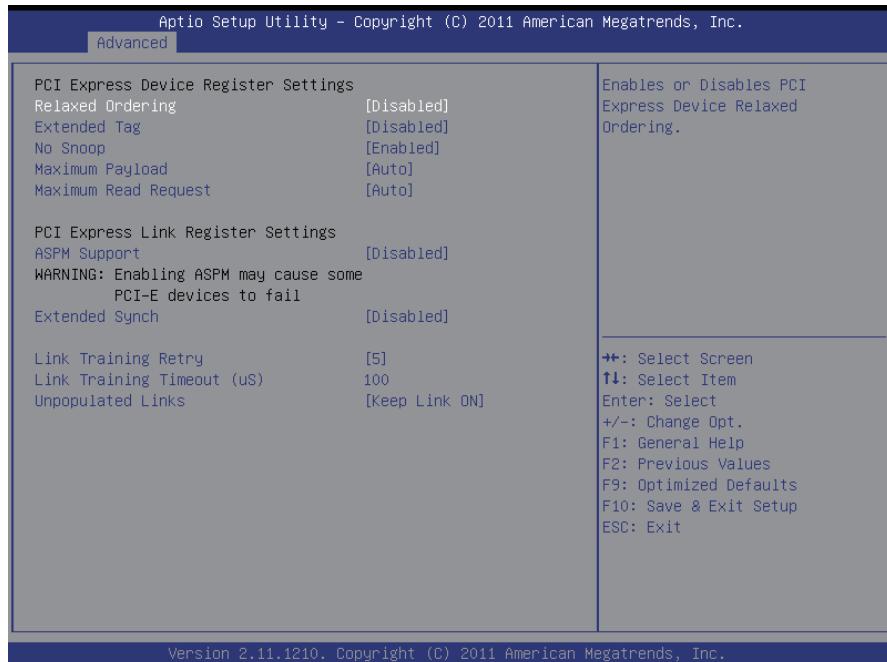
PERR# Generation

Enables or Disables PCI Device to Generate PERR#.

SERR# Generation

Enables or Disables PCI Device to Generate SERR#.

PCI Express Settings



Relaxed Ordering

Enables or Disables PCI Express Device Relaxed ordering.

Extended Tag

If Enabled, allows Device to use 8-bit Tag field as a requester.

No Snoop

Enables or Disables PCI Express Device No Snoop Option.

Maximum Payload

Set Maximum Payload of PCI Express Device or allow System BIOS to select the value.

The choice: Auto, 128 bytes, 256 bytes, 512 bytes, 1024 bytes, 2048 bytes, 4096 bytes

Maximum Read Request

Set Maximum Read Request of PCI Express Device or allow System BIOS to select the value.

The choice: Auto, 128 bytes, 256 bytes, 512 bytes, 1024 bytes, 2048 bytes, 4096 bytes

ASPM Support

Set the ASPM Level:

- Force L0s: Force all links to L0s State
- AUTO: BIOS auto configure:
- DISABLE: Disables ASPM.

Extended Synch

If Enabled, allows generation of Extended Synchronization patterns.

Link Training Retry

Defines number of Retry Attempts software will take to retrain the link if previous training attempt was unsuccessful.

The choice: Disabled, 2, 3, 5

Link Training Timeout (uS)

Defines number of Microseconds software will wait before polling “Link Training” bit in Link Status register. Value ranges from 1 to 100 uS.

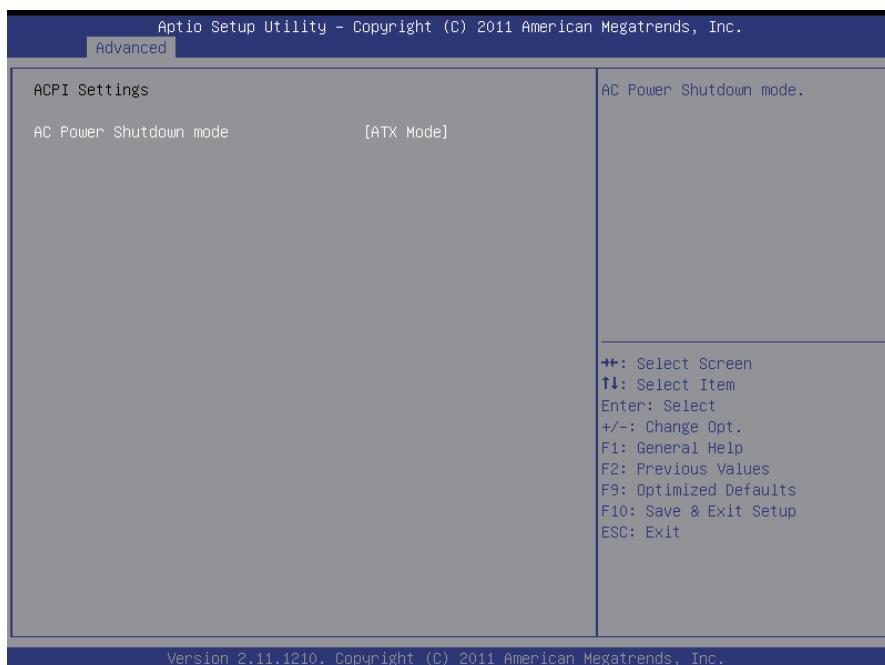
The choice: 1~100

Unpopulated Links

In order to save power, software will disable unpopulated PCI Express links, if this option is set to “Disable Link”.

The choice: Keep Link ON, Disable Link

3.2.2 ACPI Settings



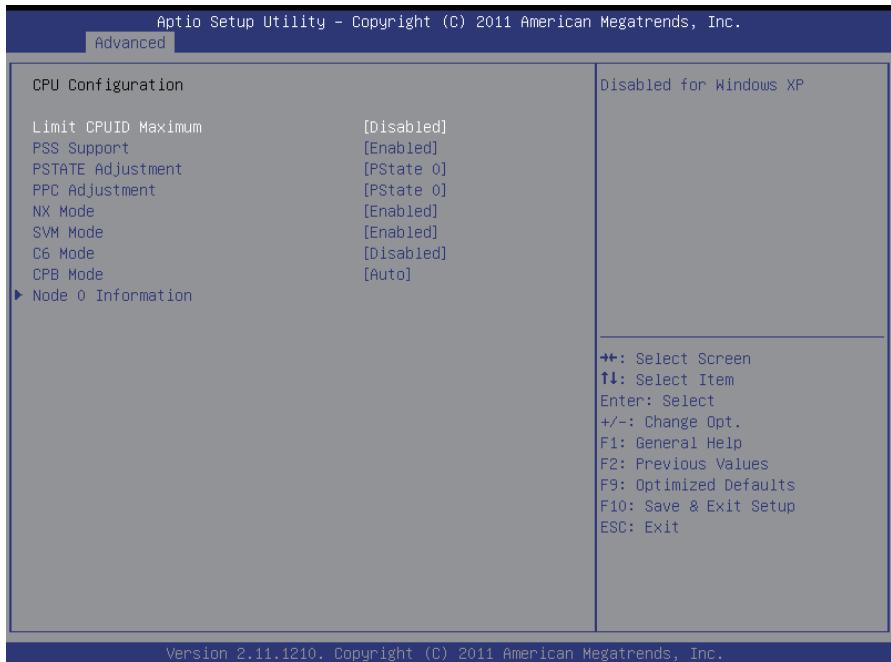
AC Power Shutdown mode

Choose AC Power Shutdown mode.

The choice: AT Mode, ATX Mode

3.2.3 CPU Configuration

The CPU Configuration setup screen varies depending on the installed processor.



Limit CPUID Maximum

Disabled for Windows XP.

PSS Support

Enable/Disable the generation of ACPI _PPC, _PPS, and _PCT objects.

PSATATE Adjustment

Provide to adjust startup P-state level.

The choice: PState 0, PState 1, PState 2

PPC Adjustment

Provide to adjust _PPC object.

The choice: PState 0, PState 1, PState 2

NX Mode

Enable/Disable No-execute page protection Function.

SVM Mode

Enable/Disable CPU Virtualization.

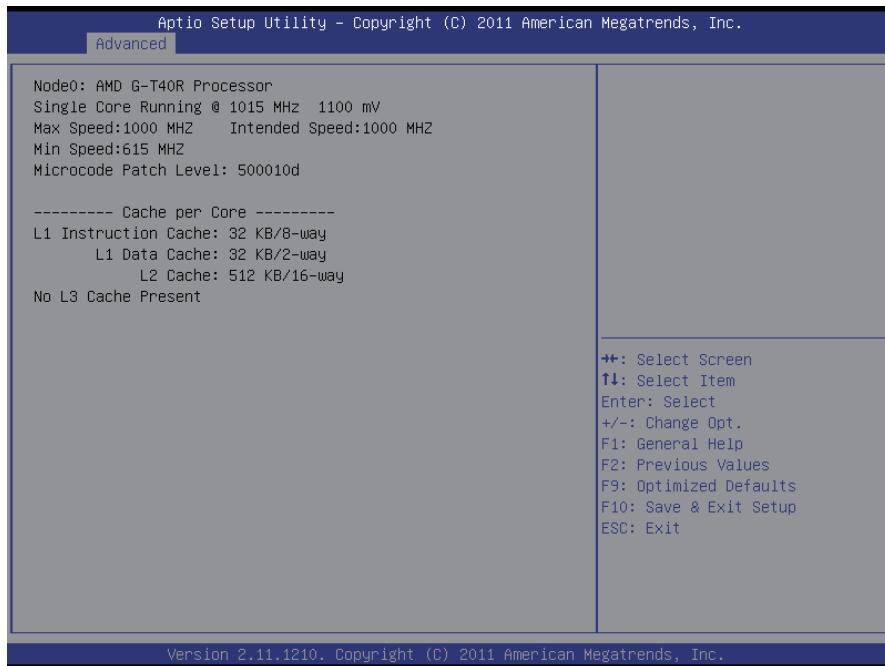
C6 Mode

Enable/Disable C6.

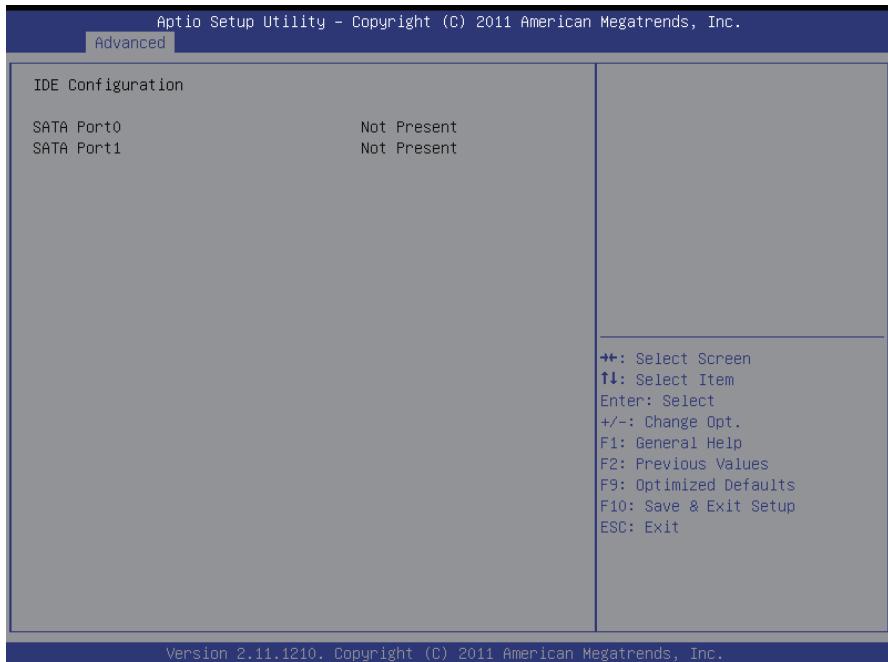
CPB Mode

Auto/disable CPB.

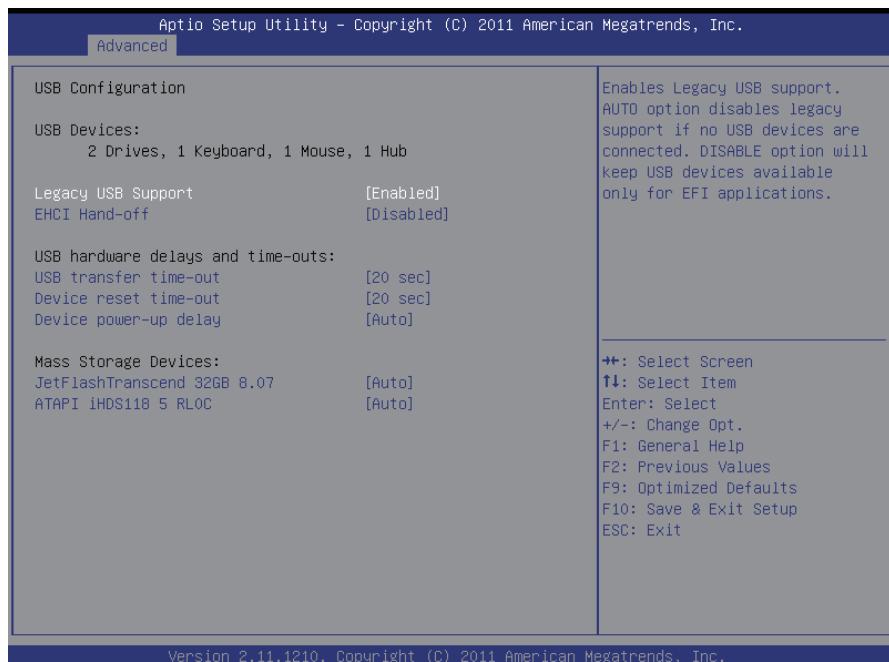
Node 0 Information



3.2.4 IDE Configuration



3.2.5 USB Configuration



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Legacy USB Support

Enable Legacy USB support. AUTO option disables legacy support if no USB devices are connected. DISABLE option will keep USB devices available only for EFI applications.

The choice: Enabled (Default); Auto; Disabled

EHCI Hand-off

Allow you to enable support for operating systems without an EHCI hand-off feature. Do not disable the BIOS EHCI Hand-Off option if you are running a Windows® operating system with USB device.

The choice: Enabled (Default); Disabled

USB hardware delays and time-outs

USB transfer time-out — The time-out value for control, bulk, and interrupt transfers. Default setting: 20 sec

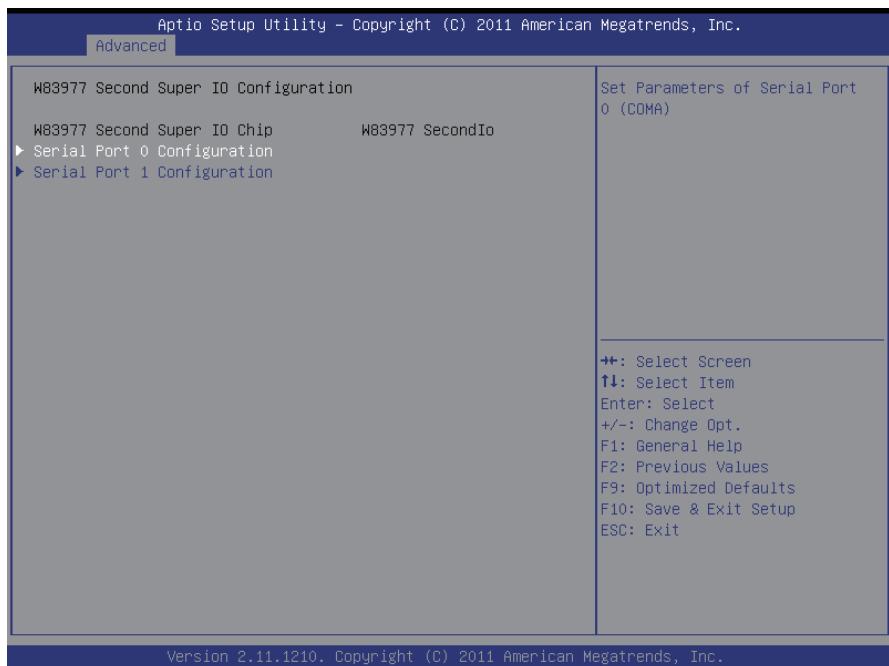
Device reset time-out — USB mass storage device start unit command time-out. Default setting: 20 sec

Device power-up delay — Maximum time the device will take before it properly reports itself to the host controller. ‘Auto’ uses default value: for a Root port it is 100ms, for a Hub port the delay is taken from hub descriptor. The choice: Auto (Default); Manual

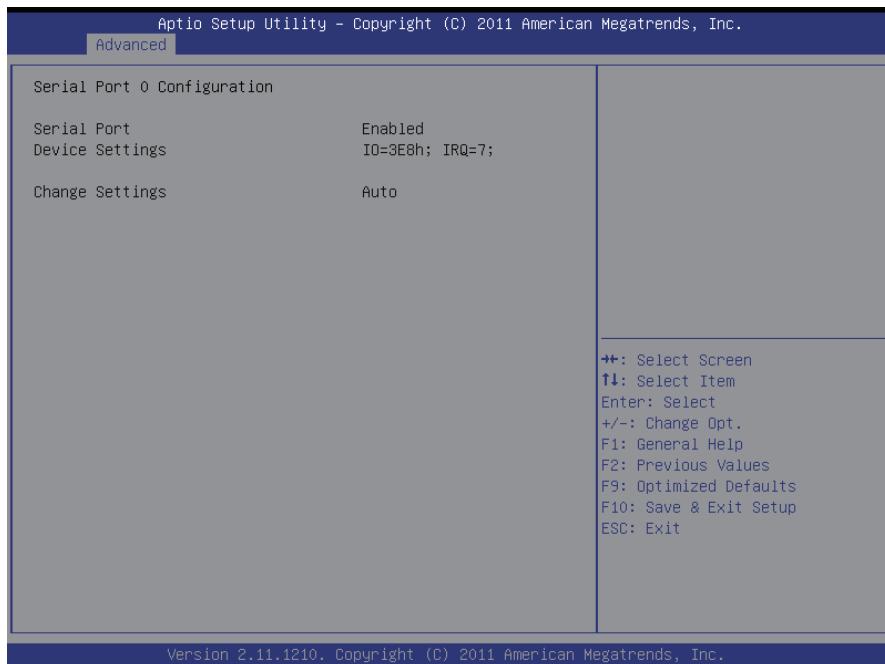
Mass Storage Devices

This item displays information when USB devices are detected.

3.2.6 W83977 Second Super IO Configuration



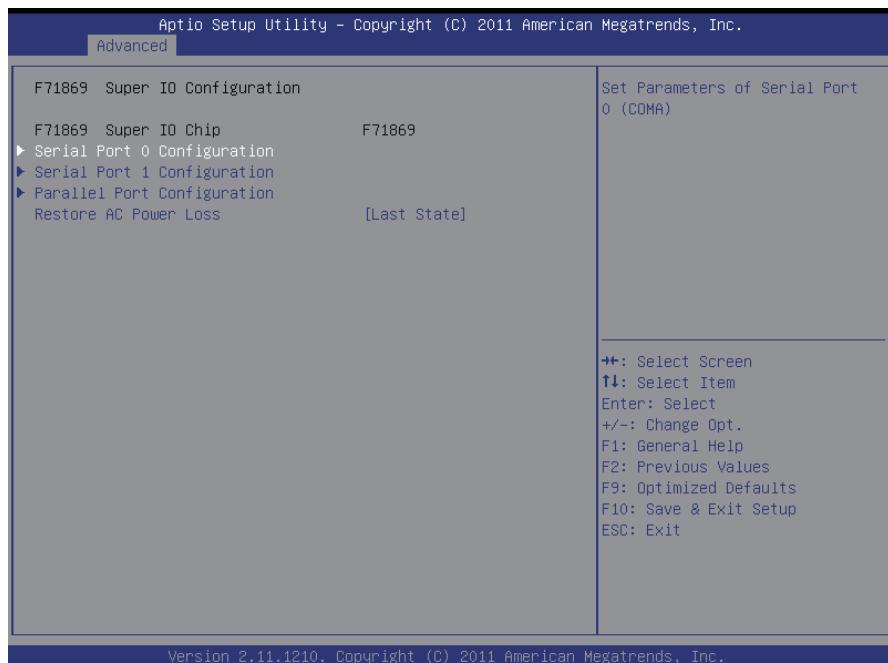
Serial Port 0 Configuration



Serial Port 1 Configuration



3.2.7 F71869 Super IO Configuration



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Restore AC Power Loss

Select Restore AC Power Loss mode.

The choice: Last State, Always On, Bypass Mode, Always Off

Serial/Parallel Port 0/1 Configuration



Serial Port

Use the Serial port option to enable or disable the serial port.

The choice: Enabled, Disabled

Change Settings

Use the Change Settings option to change the serial port's IO port address and interrupt address.

The choice:

Auto

IO=3F8h; IRQ=4,

IO=3F8h; IRQ=3,4,5,6,7,10,11,12

IO=2F8h; IRQ=3,4,5,6,7,10,11,12

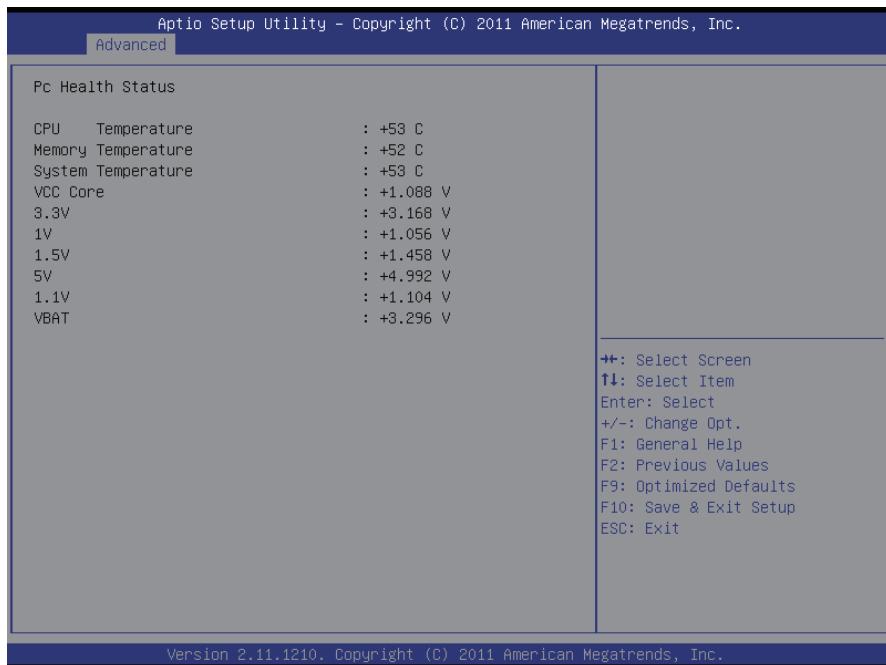
IO=3E8h; IRQ=3,4,5,6,7,10,11,12

IO=2E8h; IRQ=3,4,5,6,7,10,11,12

Device Mode (Except Serial Port 0 Configuration)

The choice: Standard Parallel Port Mode, EPP Mode, ECP Mode, EPP Mode & ECP Mode.

3.2.8 F71869 H/W Monitor



3.2.9 Wake Event



Wake On Lan

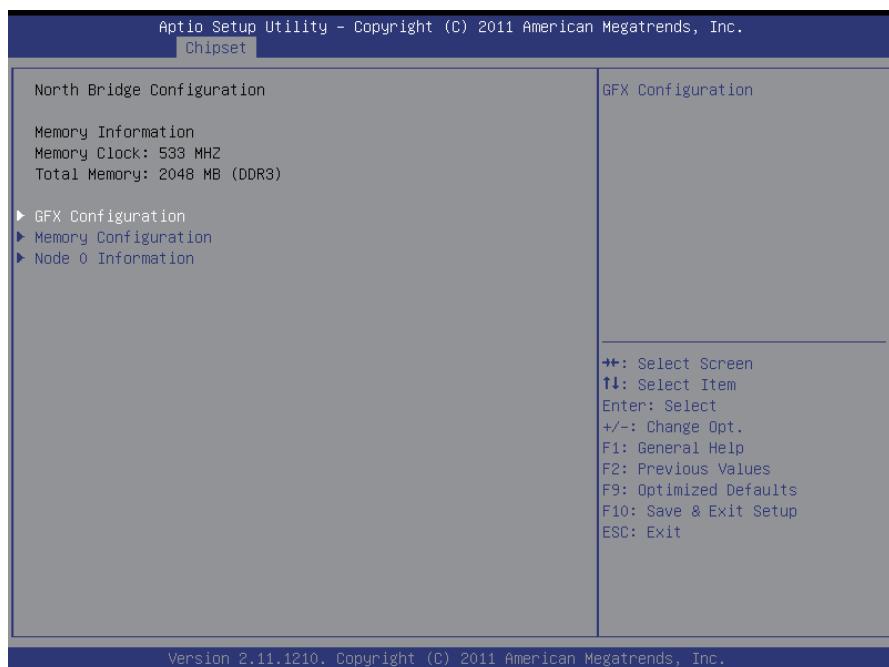
Enable/Disable Wake On Lan help.

3.3 Chipset

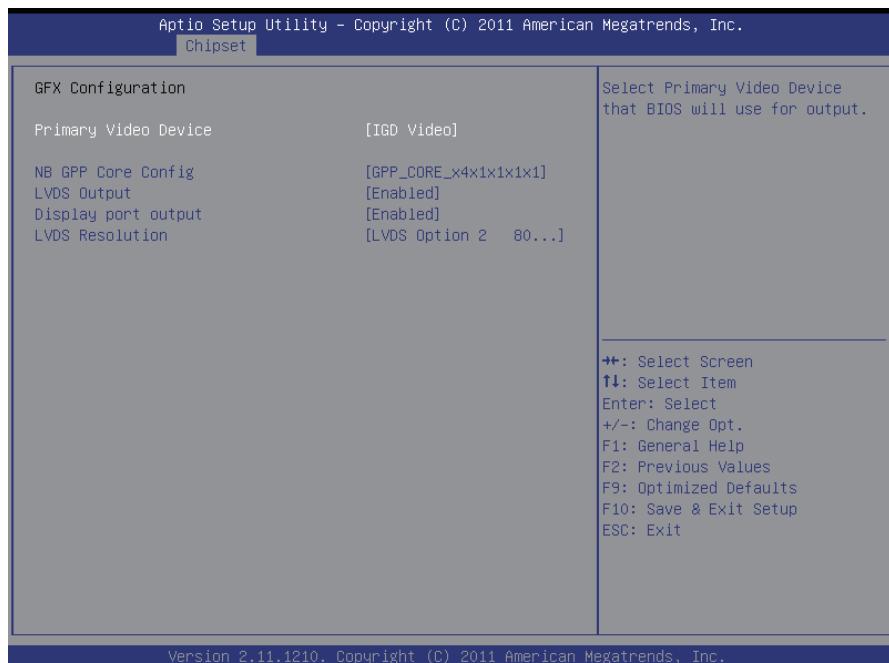
This section allows you to configure and improve your system; also, set up some system features according to your preference.



3.3.1 North Bridge



GFX Configuration



Primary Video Device

Select Primary Video Device that BIOS will use for output.

NB GPP Core Config

Configure NB GPP Core.

The choice: Disabled, GPP_CORE_x4x4, GPP_CORE_x4x2x2, GPP_CORE_x4x2x1x1, GPP_CORE_x4x1x1x1

LVDS Output

Enable/Disable NB PCIe Connect Type (Display type).

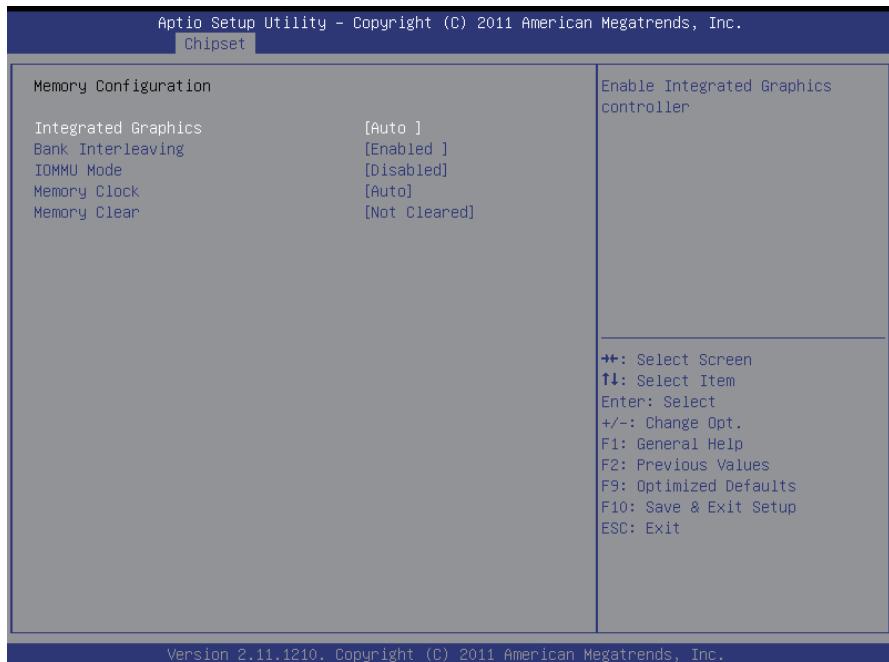
Display port output

Enable/Disable NB PCIe Connect Type (Display type).

LVDS Resolution

Set LVDS Resolution.

Memory Configuration



Integrated Graphics

The Integrated Graphics controller configuration is set to Auto.

The choice: Disabled, Force, Auto

Bank Interleaving

The choice: Disabled, Enabled

IOMMU Mode

IOMMU is supported on LINUX based systems to convert 32bit I/O to 64bit MMIO.

Memory Clock

This item allows user to select different memory clock.

Memory Clear

This is for memory clear functionality control.

Node 0 Information

Aptio Setup Utility - Copyright (C) 2011 American Megatrends, Inc.

Chipset

Node 0 Information

Starting Address: 0KB
Ending Address: 2097151KB

Dimm0: size = 2048MB, speed = 667MHz
Dimm1: Not Present

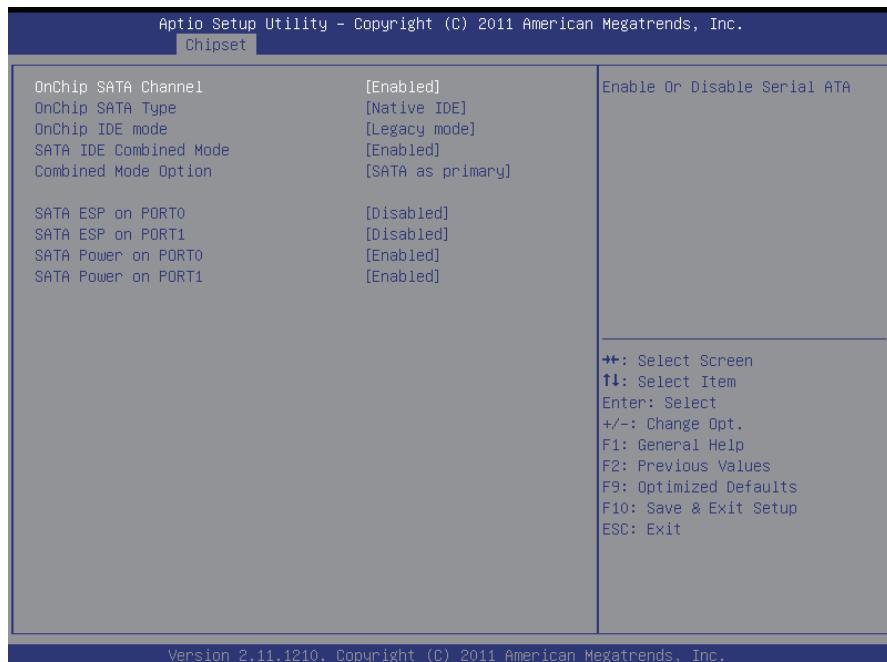
++: Select Screen
↓↑: Select Item
Enter: Select
+/-: Change Opt.
F1: General Help
F2: Previous Values
F9: Optimized Defaults
F10: Save & Exit Setup
ESC: Exit

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3.3.2 South Bridge



SB SATA Configuration



OnChip SATA Channel

Enable/Disable Serial ATA.

OnChip SATA Type

The choice: Native IDE, RAID, AHCI, Legacy IDE, IDE→AHCI, AHCI as ID 0x4394, IDE→AHCI as ID 0x4394

OnChip IDE mode

OnChip IDE mode Select.

The choice: Legacy mode, Native mode

SATA IDE Combined Mode

Enable/Disable SATA IDE Combined Mode.

Combined Mode Option

The choice: SATA as primary, SATA as secondary

SATA ESP on PORT0/1

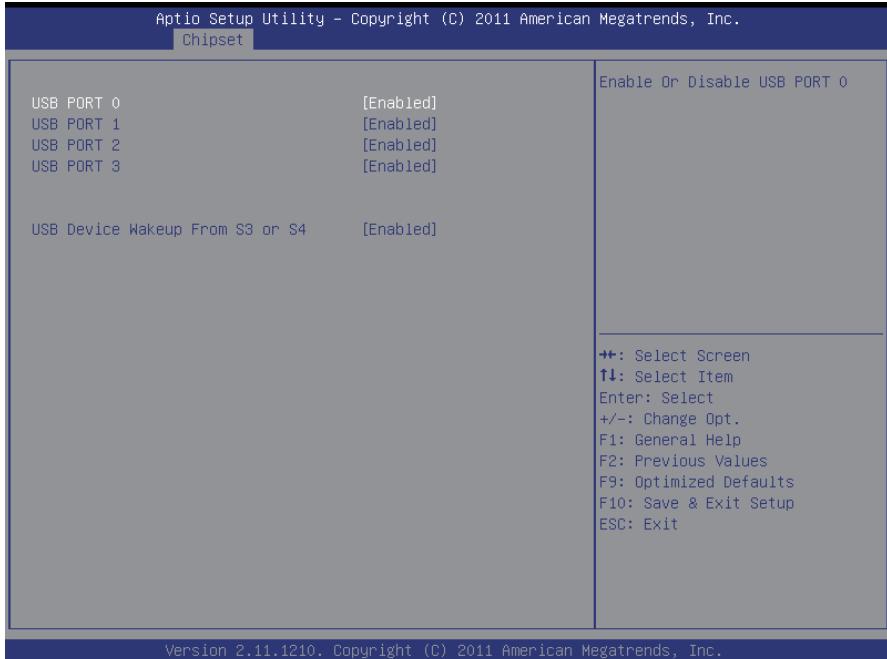
Enable/Disable SATA ESP on PORT0/1.

SATA Power on PORT0/1

Enable/Disable SATA Power on PORT0/1.

The choice: Enabled, Power Down

SB USB Configuration



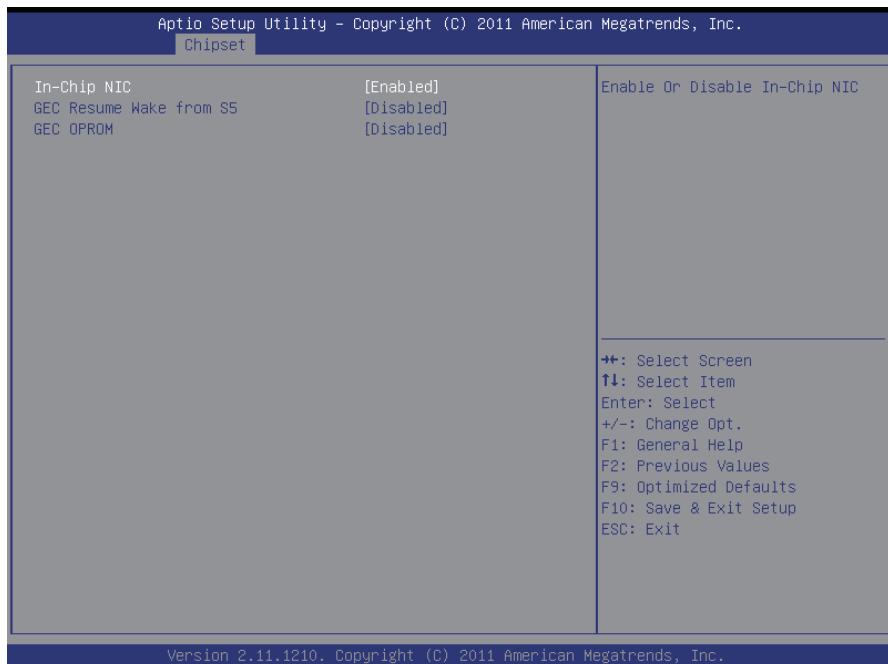
USB PORT 0~3

Enable/Disable USB PORT 0~13/FL0~1.

USB Device Wakeup From S3 or S4

Enable/Disable USB Device Wakeup From S3 or S4.

SB GEC Configuration



In-Chip NIC

Enable/Disable In-Chip NIC.

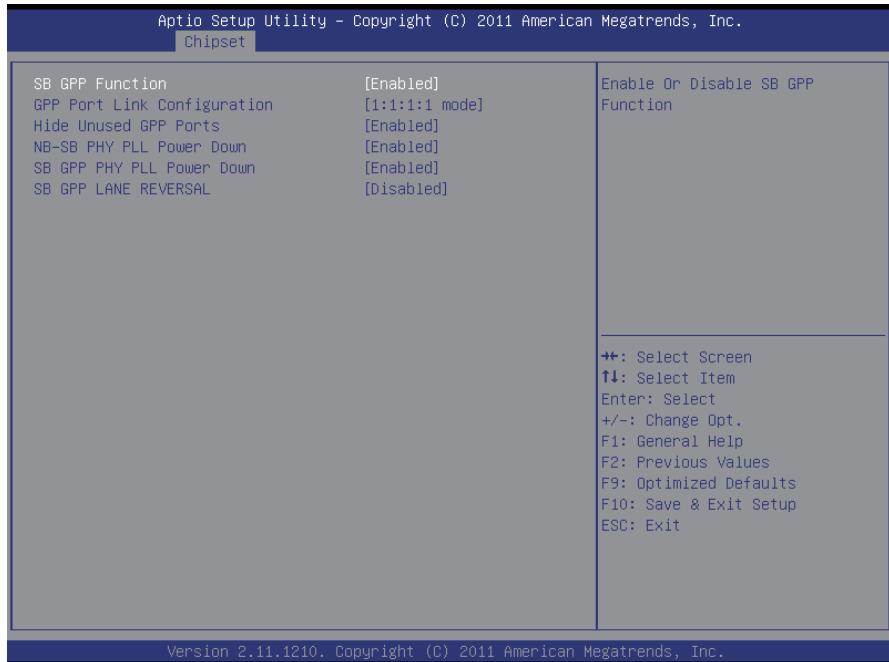
GEC Resume Wake from S5

Enable/Disable GEC Resume Wake from S5.

GEC OPROM

Enable/Disable GEC OPROM.

SB GPP Port Configuration



SB GPP Function

Enable/Disable SB GPP Function.

GPP Port Link Configuration

Select GPP Port Link Configuration.

Hide Unused GPP Ports

Enable/Disable Hide Unused GPP Ports.

NB-SB PHY PLL Power Down

Enable/Disable NB-SB PHY PLL Power Down.

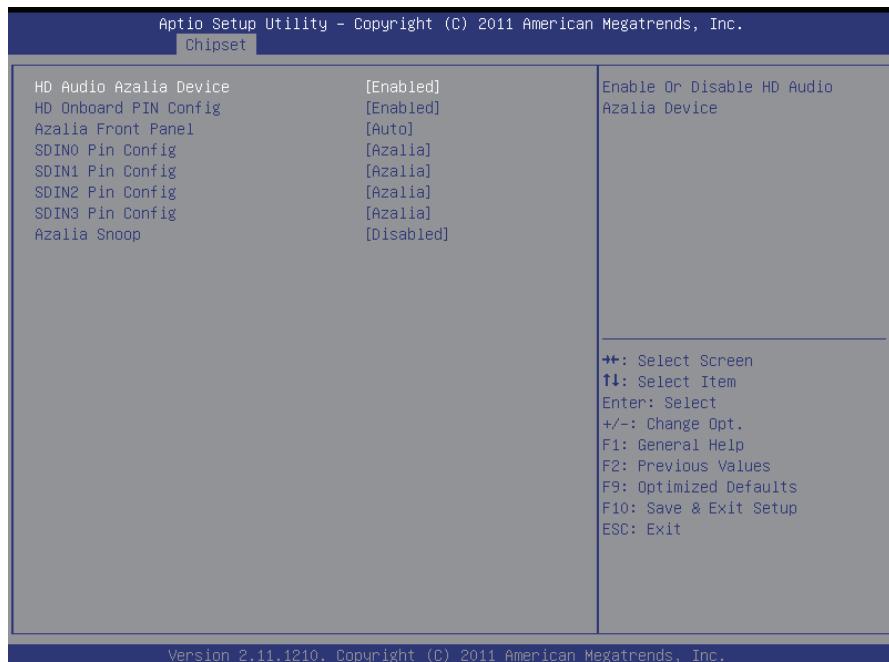
SB GPP PHY PLL Power Down

Enable/Disable SB GPP PHY PLL Power Down.

SB GPP LANE REVERSAL

Enable/Disable SB GPP LANE REVERSAL.

SB HD Azalia Configuration



HD Audio Azalia Device

The choice: Auto, Disabled, Enabled

HD Onboard PIN Config

The choice: Disabled, Enabled

Azalia Front Panel

The choice: Auto, Disabled

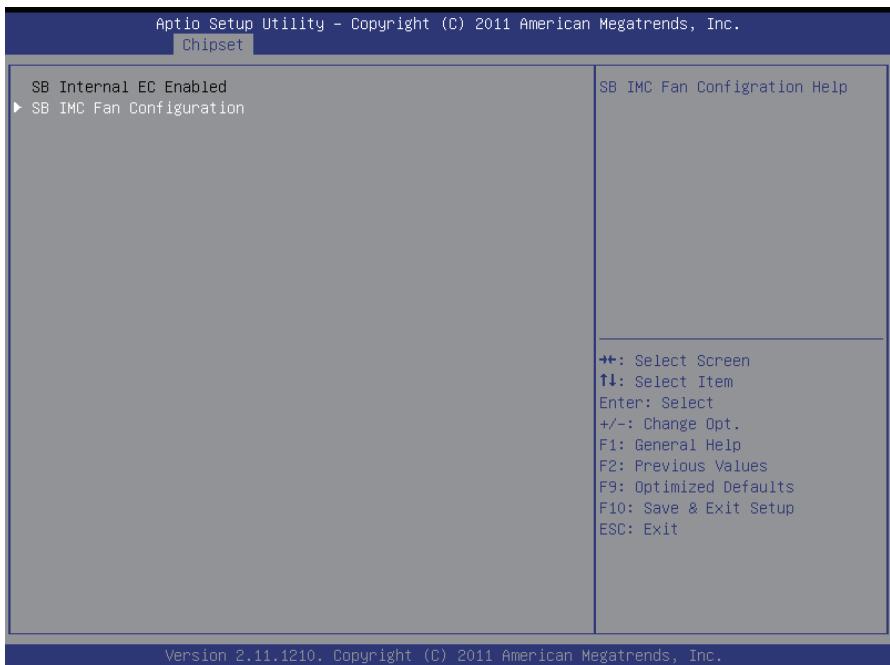
SDIN0~3 PIN Config

The choice: GPIO, Azalia

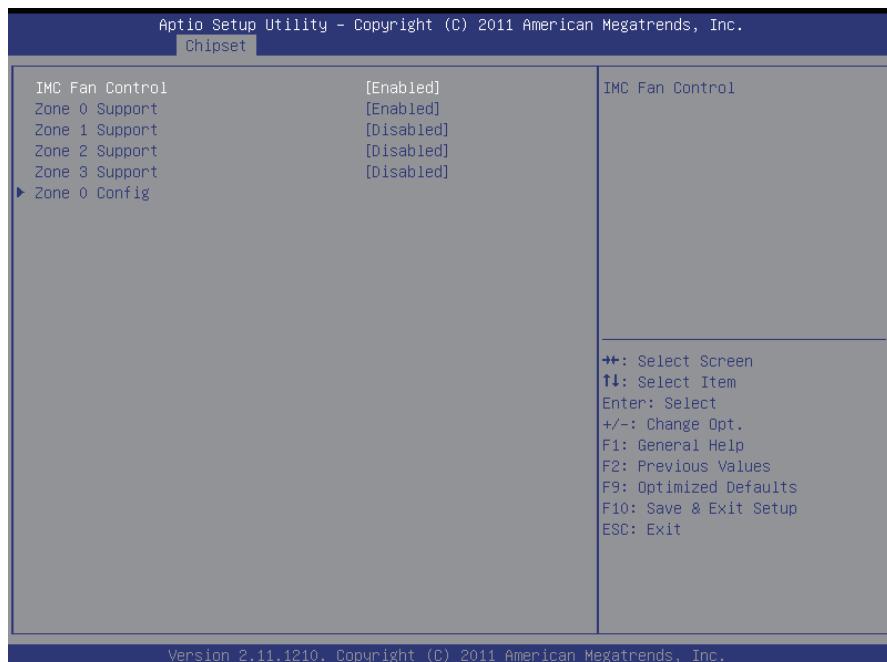
Azalia Snoop

The choice: Disabled, Enabled

EC Configuration



SB IMC Fan Configuration



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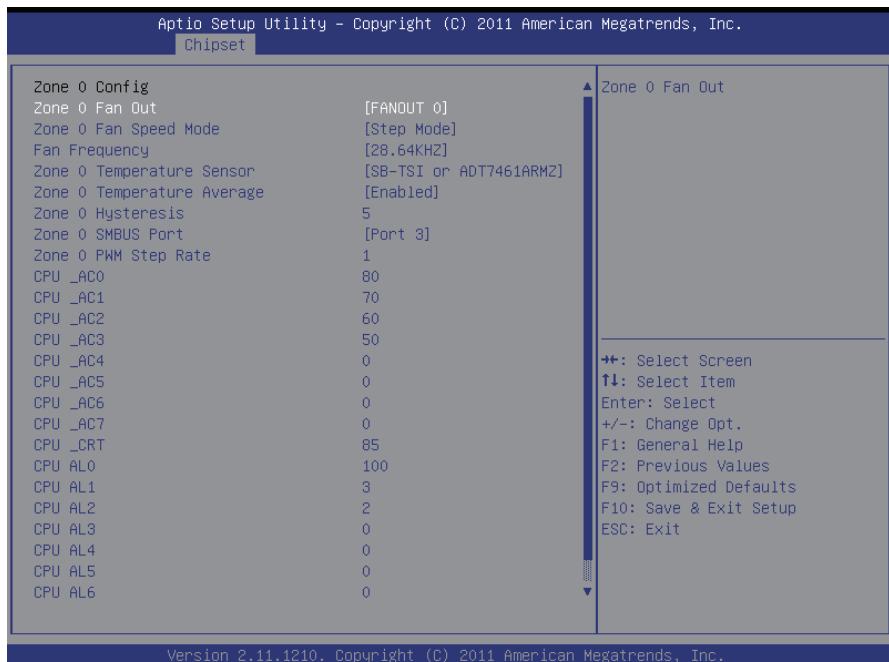
IMC Fan Control

The choice: Disabled, Enabled

Zone 0~3 Support

The choice: Disabled, Enabled

Zone 0 Config



Zone 0 Fan Out

The choice: No Fan, FANOUT 0~4

Zone 0 Fan Speed Mode

The choice: Linear Mode, Step Mode

Fan Frequency

Set fan frequency.

Zone 0 Temperature Sensor

The choice: No Sensor, TEMPIN 0~3, Int TEMP, SB-TSI or ADT7461ARMZ, ADM1032 or ADT7461ARM

Zone 0 Temperature Average

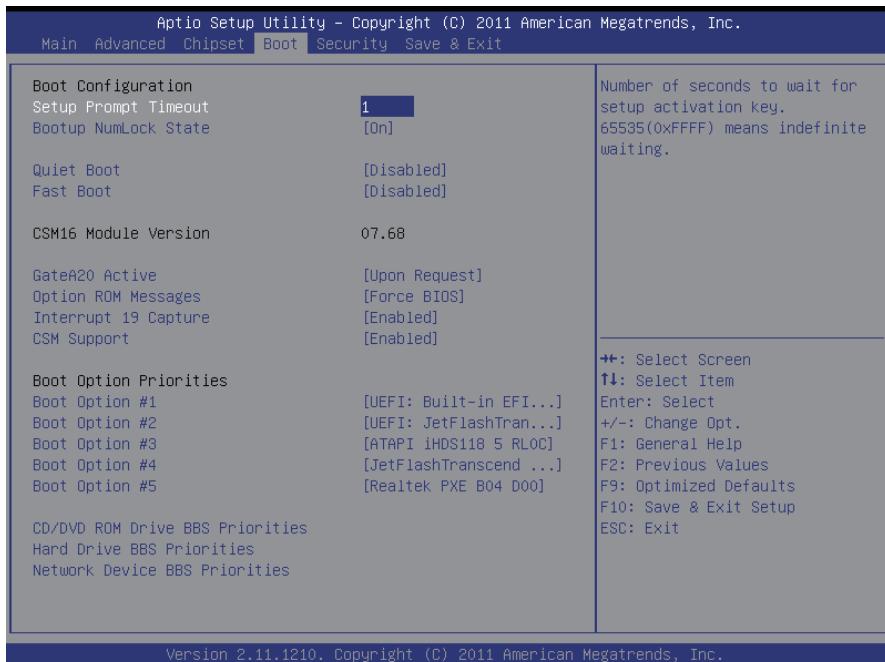
The choice: Disabled. Enabled

Zone 0 SMBUS Port

The choice: Port 0/2~4

3.4 Boot Settings

The Boot menu items allow you to change the system boot options.



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Boot Configuration

Setup Prompt Timeout

Seconds to wait for setup activation key. 65535(0xFFFF) means indefinite waiting.

Bootup NumLock State

This setting determines whether the Num Lock key should be activated at boot up.

Quiet Boot

This allows you to select the screen display when the system boots.

Fast Boot

Enable/Disable boot with initialization of a minimal set of devices required to launch active boot option. Has no effect for BBS boot options.

GateA20 Active

This item is to set the Gate A20 status.

Option ROM Messages

This item is to set display mode for Option ROM.

Interrupt 19 Capture

When enabled, it allows the optional ROM to trap interrupt 19.

CSM Support

Enabled/ disabled CSM support. If Auto is selected, based on OS, CSM will be enabled/ disabled automatically.

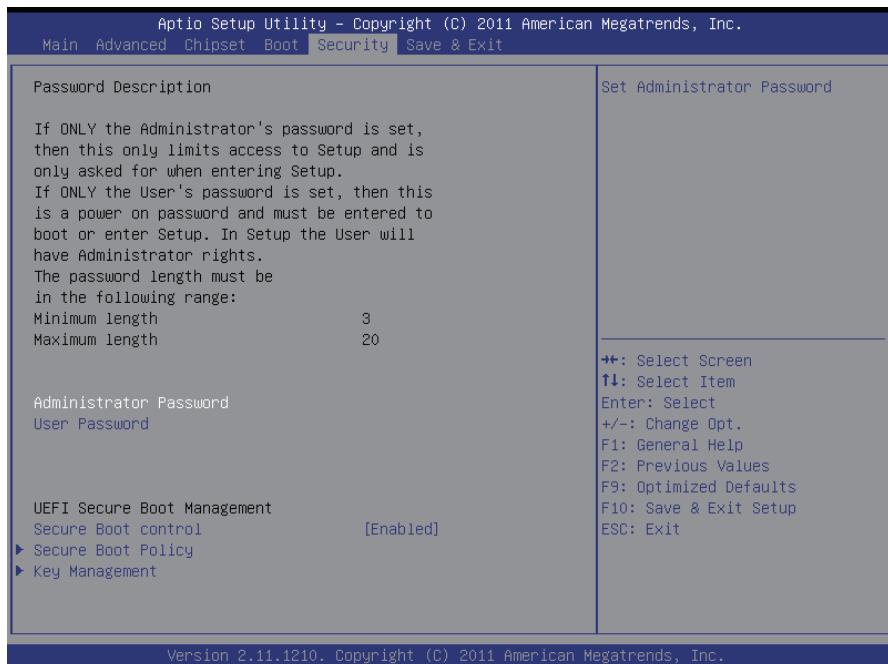
Boot Option Priorities

Select the boot sequence of the hard drives.

Network Device BBS Priorities

This option sets the order of the legacy devices in this group.

3.5 Security



Administrator Password

Use this feature to set the Administrator Password which is required to enter the BIOS setup utility. The length of the password should be from 3-characters to 8-characters long.

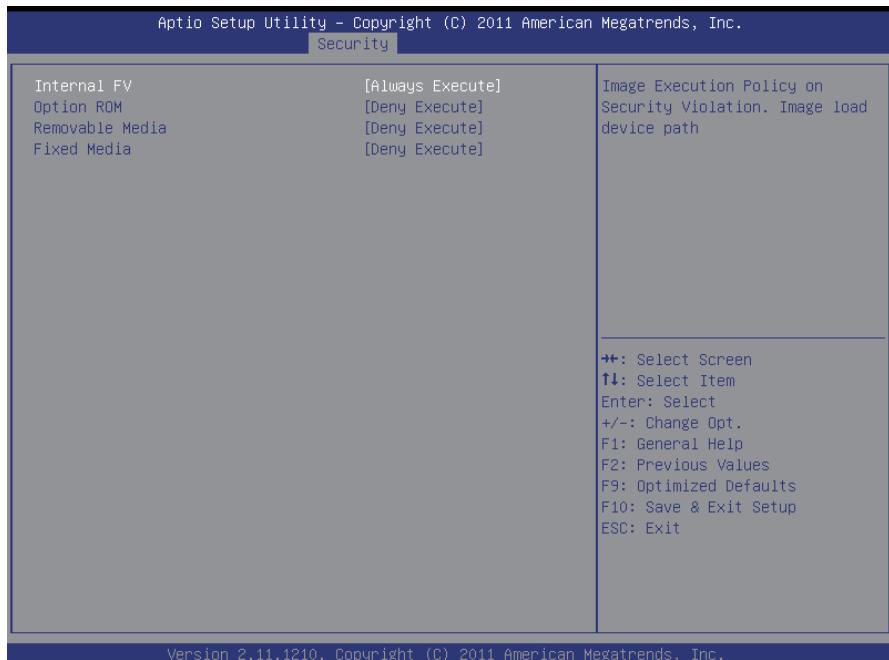
User Password

Use this feature to set a User Password which is required to log into the system and to enter the BIOS setup utility. The length of the password should be from 3-characters to 8-characters long.

CSM Support

Enabled/ disabled CSM support. If Auto is selected, based on OS, CSM will be enabled/ disabled automatically.

Secure Boot Policy

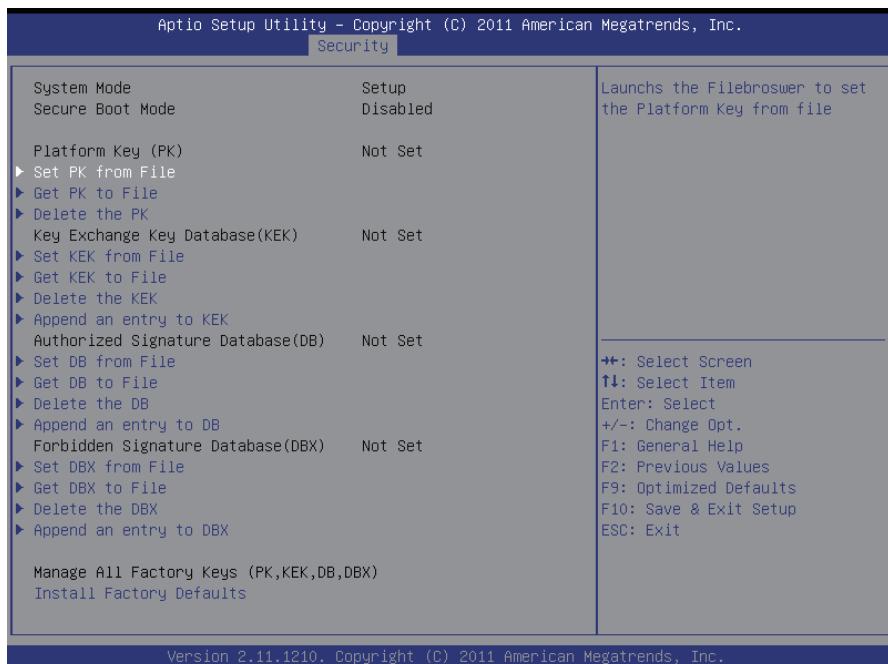


Internal FV/ Option ROM/ Removable Media/ Fixed Media

Image Execution Policy on Security Violation. Image load device path.

The choice: Always Execute, Always Execute, Allow Execute, Defer Execute, Deny Execute, Query User

Key Management



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Set PK from File

Launches the Filebrowser to set the Platform Key from file.

Get PK to File

Stores the existing Platform Key to file name OK in selected file system's root.

Delete the PK

Deletes the Platform Key.

Set KEK to File

Launches the Filebrowser to set the Key Exchange Key Signature Database from file.

Get KEK to File

Stores the existing Key Exchange Key Signature Database to file name KEK in selected file system's root.

Delete the KEK

Deletes the Key Exchange Key Signature Database.

Append an entry to KEK

Launches the Filebrowser to Append the Key Exchange Key Signature Database entry from file.

Set DB from File

Launches the Filebrowser to set the Authorized Signature Database from file.

Get DB to File

Stores the existing Authorized Signature Database to file name DB in selected file system's root.

Delete the DB

Deletes the Authorized Signature Database.

Append an entry to DB

Launches the Filebrowser to Append the Authorized Security Database entry from file.

Set DBX from File

Launches the Filebrowser to set the Forbidden Signature Database from file.

Get DBX to File

Stores the existing Forbidden Signature Database to file name DB in selected file system's root.

Delete the DBX

Deletes the Forbidden Signature Database.

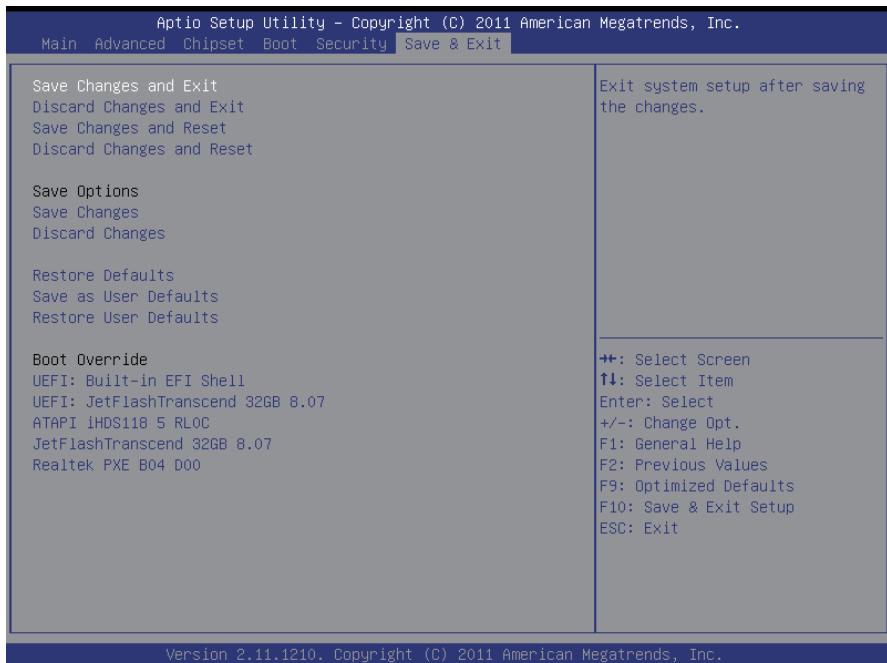
Append an entry to DBX

Launches the Filebrowser to Append the Forbidden Signature Database entry from file.

Install Factory Defaults

Set Default Secure Variables: PK-KEK-db-dbx. Change takes effect on next reboot.

3.6 Save & Exit



Save Changes and Exit

Pressing <Enter> on this item and it asks for confirmation:

Save configuration changes and exit setup?

Pressing <OK> stores the selection made in the menus in CMOS - a special section of memory that stays on after you turn your system off. The next time you boot your computer, the BIOS configures your system according to the Setup selections stored in CMOS. After saving the values the system is restarted again.

Discard Changes and Exit

Exit system setup without saving any changes.
<ESC> key can be used for this operation.

Save Changes and Reset

Reset the system after saving the changes.

Discard Changes and Reset

Reset system setup without saving any changes.

Save Changes

Save changes done so far to any of the setup options.

Discard Changes

Discard changes done so far to any of the setup options.

Restore Defaults

Restore system to factory default.

Pressing <Enter> on this item and it asks for confirmation prior to executing this command.

Save as User Defaults

Save the changes done so far as User Defaults.

Restore User Defaults

Restore the User Defaults to all the setup options.

Boot Override

This group of functions includes a list of tokens, each of them corresponding to one device within the boot order. Select a drive to immediately boot that device regardless of the current boot order.

3.7 AMI BIOS Checkpoints

3.7.1 Checkpoint Ranges

Status Code Range	Description
0x01 – 0x0B	SEC execution
0x0C – 0x0F	SEC errors
0x10 – 0x2F	PEI execution up to and including memory detection
0x30 – 0x4F	PEI execution after memory detection
0x50 – 0x5F	PEI errors
0x60 – 0x8F	DXE execution up to BDS
0x90 – 0xCF	BDS execution
0xD0 – 0xDF	DXE errors
0xE0 – 0xE8	S3 Resume (PEI)
0xE9 – 0xEF	S3 Resume errors (PEI)
0xF0 – 0xF8	Recovery (PEI)
0xF9 – 0xFF	Recovery errors (PEI)

3.7.2 Standard Checkpoints

SEC Phase

Status Code	Description
0x00	Not used
Progress Codes	
0x01	Power on. Reset type detection (soft/hard).
0x02	AP initialization before microcode loading
0x03	North Bridge initialization before microcode loading
0x04	South Bridge initialization before microcode loading
0x05	OEM initialization before microcode loading
0x06	Microcode loading
0x07	AP initialization after microcode loading
0x08	North Bridge initialization after microcode loading
0x09	South Bridge initialization after microcode loading
0x0A	OEM initialization after microcode loading
0x0B	Cache initialization
SEC Error Codes	
0x0C – 0x0D	Reserved for future AMI SEC error codes
0x0E	Microcode not found
0x0F	Microcode not loaded

PEI Phase

Status Code	Description
Progress Codes	
0x10	PEI Core is started
0x11	Pre-memory CPU initialization is started
0x12	Pre-memory CPU initialization (CPU module specific)
0x13	Pre-memory CPU initialization (CPU module specific)
0x14	Pre-memory CPU initialization (CPU module specific)
0x15	Pre-memory North Bridge initialization is started
0x16	Pre-Memory North Bridge initialization (North Bridge module specific)
0x17	Pre-Memory North Bridge initialization (North Bridge module specific)
0x18	Pre-Memory North Bridge initialization (North Bridge module specific)
0x19	Pre-memory South Bridge initialization is started
0x1A	Pre-memory South Bridge initialization (South Bridge module specific)
0x1B	Pre-memory South Bridge initialization (South Bridge module specific)
0x1C	Pre-memory South Bridge initialization (South Bridge module specific)
0x1D – 0x2A	OEM pre-memory initialization codes
0x2B	Memory initialization. Serial Presence Detect (SPD) data reading
0x2C	Memory initialization. Memory presence detection
0x2D	Memory initialization. Programming memory timing information
0x2E	Memory initialization. Configuring memory
0x2F	Memory initialization (other).
0x30	Reserved for ASL (see ASL Status Codes section below)
0x31	Memory Installed

BIOS

0x32	CPU post-memory initialization is started
0x33	CPU post-memory initialization. Cache initialization
0x34	CPU post-memory initialization. Application Processor(s) (AP) initialization
0x35	CPU post-memory initialization. Boot Strap Processor (BSP) selection
0x36	CPU post-memory initialization. System Management Mode (SMM) initialization
0x37	Post-Memory North Bridge initialization is started
0x38	Post-Memory North Bridge initialization (North Bridge module specific)
0x39	Post-Memory North Bridge initialization (North Bridge module specific)
0x3A	Post-Memory North Bridge initialization (North Bridge module specific)
0x3B	Post-Memory South Bridge initialization is started
0x3C	Post-Memory South Bridge initialization (South Bridge module specific)
0x3D	Post-Memory South Bridge initialization (South Bridge module specific)
0x3E	Post-Memory South Bridge initialization (South Bridge module specific)
0x3F-0x4E	OEM post memory initialization codes
0x4F	DXE IPL is started

PEI Error Codes

0x50	Memory initialization error. Invalid memory type or incompatible memory speed
0x51	Memory initialization error. SPD reading has failed
0x52	Memory initialization error. Invalid memory size or memory modules do not match.
0x53	Memory initialization error. No usable memory detected
0x54	Unspecified memory initialization error.

0x55	Memory not installed
0x56	Invalid CPU type or Speed
0x57	CPU mismatch
0x58	CPU self test failed or possible CPU cache error
0x59	CPU micro-code is not found or micro-code update is failed
0x5A	Internal CPU error
0x5B	reset PPI is not available
0x5C-0x5F	Reserved for future AMI error codes

S3 Resume Progress Codes

0xE0	S3 Resume is started (S3 Resume PPI is called by the DXE IPL)
0xE1	S3 Boot Script execution
0xE2	Video repost
0xE3	OS S3 wake vector call
0xE4-0xEF	Reserved for future AMI progress codes

S3 Resume Error Codes

0xE8	S3 Resume Failed
0xE9	S3 Resume PPI not Found
0xEA	S3 Resume Boot Script Error
0xEB	S3 OS Wake Error
0xEC-0xEF	Reserved for future AMI error codes

Recovery Progress Codes

0xF0	Recovery condition triggered by firmware (Auto recovery)
0xF1	Recovery condition triggered by user (Forced recovery)
0xF2	Recovery process started
0xF3	Recovery firmware image is found
0xF4	Recovery firmware image is loaded
0xF5-0xF7	Reserved for future AMI progress codes

Recovery Error Codes

0xF8	Recovery PPI is not available
------	-------------------------------

0xF9	Recovery capsule is not found
0xFA	Invalid recovery capsule
0xFB – 0xFF	Reserved for future AMI error codes

DXE Phase

Status Code	Description
0x60	DXE Core is started
0x61	NVRAM initialization
0x62	Installation of the South Bridge Runtime Services
0x63	CPU DXE initialization is started
0x64	CPU DXE initialization (CPU module specific)
0x65	CPU DXE initialization (CPU module specific)
0x66	CPU DXE initialization (CPU module specific)
0x67	CPU DXE initialization (CPU module specific)
0x68	PCI host bridge initialization
0x69	North Bridge DXE initialization is started
0x6A	North Bridge DXE SMM initialization is started
0x6B	North Bridge DXE initialization (North Bridge module specific)
0x6C	North Bridge DXE initialization (North Bridge module specific)
0x6D	North Bridge DXE initialization (North Bridge module specific)
0x6E	North Bridge DXE initialization (North Bridge module specific)
0x6F	North Bridge DXE initialization (North Bridge module specific)
0x70	South Bridge DXE initialization is started
0x71	South Bridge DXE SMM initialization is started
0x72	South Bridge devices initialization
0x73	South Bridge DXE Initialization (South Bridge module specific)

0x74	South Bridge DXE Initialization (South Bridge module specific)
0x75	South Bridge DXE Initialization (South Bridge module specific)
0x76	South Bridge DXE Initialization (South Bridge module specific)
0x77	South Bridge DXE Initialization (South Bridge module specific)
0x78	ACPI module initialization
0x79	CSM initialization
0x7A – 0x7F	Reserved for future AMI DXE codes
0x80 – 0x8F	OEM DXE initialization codes
0x90	Boot Device Selection (BDS) phase is started
0x91	Driver connecting is started
0x92	PCI Bus initialization is started
0x93	PCI Bus Hot Plug Controller Initialization
0x94	PCI Bus Enumeration
0x95	PCI Bus Request Resources
0x96	PCI Bus Assign Resources
0x97	Console Output devices connect
0x98	Console input devices connect
0x99	Super IO Initialization
0x9A	USB initialization is started
0x9B	USB Reset
0x9C	USB Detect
0x9D	USB Enable
0x9E – 0x9F	Reserved for future AMI codes
0xA0	IDE initialization is started
0xA1	IDE Reset
0xA2	IDE Detect
0xA3	IDE Enable

0xA4	SCSI initialization is started
0xA5	SCSI Reset
0xA6	SCSI Detect
0xA7	SCSI Enable
0xA8	Setup Verifying Password
0xA9	Start of Setup
0xAA	Reserved for ASL (see ASL Status Codes section below)
0xAB	Setup Input Wait
0xAC	Reserved for ASL (see ASL Status Codes section below)
0xAD	Ready To Boot event
0xAE	Legacy Boot event
0xAF	Exit Boot Services event
0xB0	Runtime Set Virtual Address MAP Begin
0xB1	Runtime Set Virtual Address MAP End
0xB2	Legacy Option ROM Initialization
0xB3	System Reset
0xB4	USB hot plug
0xB5	PCI bus hot plug
0xB6	Clean-up of NVRAM
0xB7	Configuration Reset (reset of NVRAM settings)
0xB8 – 0xBF	Reserved for future AMI codes
0xC0 – 0xCF	OEM BDS initialization codes

DXE Error Codes

0xD0	CPU initialization error
0xD1	North Bridge initialization error
0xD2	South Bridge initialization error
0xD3	Some of the Architectural Protocols are not available
0xD4	PCI resource allocation error. Out of Resources
0xD5	No Space for Legacy Option ROM
0xD6	No Console Output Devices are found

0xD7	No Console Input Devices are found
0xD8	Invalid password
0xD9	Error loading Boot Option (LoadImage returned error)
0xDA	Boot Option is failed (StartImage returned error)
0xDB	Flash update is failed
0xDC	Reset protocol is not available

ACPI/ASL Checkpoints

Status Code	Description
0x01	System is entering S1 sleep state
0x02	System is entering S2 sleep state
0x03	System is entering S3 sleep state
0x04	System is entering S4 sleep state
0x05	System is entering S5 sleep state
0x10	System is waking up from the S1 sleep state
0x20	System is waking up from the S2 sleep state
0x30	System is waking up from the S3 sleep state
0x40	System is waking up from the S4 sleep state
0xAC	System has transitioned into ACPI mode. Interrupt controller is in PIC mode.
0xAA	System has transitioned into ACPI mode. Interrupt controller is in APIC mode.

Appendix

Appendix A: I/O Port Address Map

Each peripheral device in the system is assigned a set of I/O port addresses which also becomes the identity of the device.

The following table lists the I/O port addresses used.

Address	Device Description
0x00000000-0x000003AF	PCI bus
0x00000000-0x000003AF	Motherboard resources
0x00000000-0x000003AF	Direct memory access controller
0x000003B0-0x000003DF	PCI bus
0x000003B0-0x000003DF	VgaSave
0x000003E0-0x00000CF7	PCI bus
0x00000D00-0x0000FFFF	PCI bus
0x0000F000-0x0000F0FF	Video Controller (VGA Compatible)
0x0000E000-0x0000EFFF	PCI standard PCI-to-PCI bridge
0x0000E000-0x0000EFFF	Standard Dual Channel PCI IDE Controller
0x0000E040-0x0000E047	Standard Dual Channel PCI IDE Controller
0x0000E030-0x0000E033	Standard Dual Channel PCI IDE Controller
0x0000E020-0x0000E027	Standard Dual Channel PCI IDE Controller
0x0000E010-0x0000E013	Standard Dual Channel PCI IDE Controller
0x0000D000-0x0000DFFF	PCI standard PCI-to-PCI bridge
0x0000D000-0x0000DFFF	Standard Dual Channel PCI IDE Controller
0x0000D040-0x0000D047	Standard Dual Channel PCI IDE Controller
0x0000D030-0x0000D033	Standard Dual Channel PCI IDE Controller
0x0000D020-0x0000D027	Standard Dual Channel PCI IDE Controller
0x0000D010-0x0000D013	Standard Dual Channel PCI IDE Controller
0x0000C000-0x0000CFFF	PCI standard PCI-to-PCI bridge
0x0000C000-0x0000CFFF	Ethernet Controller
0x0000F190-0x0000F197	Standard Dual Channel PCI IDE Controller
0x0000F180-0x0000F183	Standard Dual Channel PCI IDE Controller
0x0000F170-0x0000F177	Standard Dual Channel PCI IDE Controller
0x0000F160-0x0000F163	Standard Dual Channel PCI IDE Controller
0x0000F150-0x0000F15F	Standard Dual Channel PCI IDE Controller

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0x0000F100-0x0000F10F	Standard Dual Channel PCI IDE Controller
0x000001F0-0x000001F7	Primary IDE Channel
0x000003F6-0x000003F6	Primary IDE Channel
0x00000170-0x00000177	Secondary IDE Channel
0x00000376-0x00000376	Secondary IDE Channel
0x00000A79-0x00000A79	ISAPNP Read Data Port
0x00000279-0x00000279	ISAPNP Read Data Port
0x00000274-0x00000277	ISAPNP Read Data Port
0x0000040B-0x0000040B	Motherboard resources
0x000004D6-0x000004D6	Motherboard resources
0x00000C00-0x00000C01	Motherboard resources
0x00000C14-0x00000C14	Motherboard resources
0x00000C50-0x00000C51	Motherboard resources
0x00000C52-0x00000C52	Motherboard resources
0x00000C6C-0x00000C6C	Motherboard resources
0x00000C6F-0x00000C6F	Motherboard resources
0x00000CD0-0x00000CD1	Motherboard resources
0x00000CD2-0x00000CD3	Motherboard resources
0x00000CD4-0x00000CD5	Motherboard resources
0x00000CD6-0x00000CD7	Motherboard resources
0x00000CD8-0x00000CDF	Motherboard resources
0x00000800-0x0000089F	Motherboard resources
0x00000B20-0x00000B3F	Motherboard resources
0x00000900-0x0000090F	Motherboard resources
0x00000910-0x0000091F	Motherboard resources
0x0000FE00-0x0000FEFE	Motherboard resources
0x00000370-0x00000371	Motherboard resources
0x000003E8-0x000003EF	Communications Port (COM3)
0x000002E8-0x000002EF	Communications Port (COM4)
0x00000290-0x0000029F	Motherboard resources
0x00000060-0x00000060	Standard 101/102-Key or Microsoft Natural PS/2 Keyboard

0x00000064-0x00000064	Standard 101/102-Key or Microsoft Natural PS/2 Keyboard
0x0000003F8-0x000003FF	Communications Port (COM1)
0x0000002F8-0x000002FF	Communications Port (COM2)
0x000000378-0x0000037F	Printer Port (LPT1)
0x00000020-0x00000021	Programmable interrupt controller
0x000000A0-0x000000A1	Programmable interrupt controller
0x00000081-0x00000083	Direct memory access controller
0x00000087-0x00000087	Direct memory access controller
0x00000089-0x0000008B	Direct memory access controller
0x0000008F-0x0000008F	Direct memory access controller
0x000000C0-0x000000DF	Direct memory access controller
0x00000040-0x00000043	System timer
0x00000070-0x00000071	System CMOS/real time clock
0x00000061-0x00000061	System speaker
0x00000010-0x0000001F	Motherboard resources
0x00000022-0x0000003F	Motherboard resources
0x00000044-0x0000005F	Motherboard resources
0x00000062-0x00000063	Motherboard resources
0x00000065-0x0000006F	Motherboard resources
0x00000072-0x0000007F	Motherboard resources
0x00000080-0x00000080	Motherboard resources
0x00000084-0x00000086	Motherboard resources
0x00000088-0x00000088	Motherboard resources
0x0000008C-0x0000008E	Motherboard resources
0x00000090-0x0000009F	Motherboard resources
0x000000A2-0x000000BF	Motherboard resources
0x000000E0-0x000000EF	Motherboard resources
0x000004D0-0x000004D1	Motherboard resources
0x000000F0-0x000000FF	Numeric data processor
0x000003C0-0x000003DF	VgaSave

Appendix B: BIOS Memory Map

Address	Device Description
0xA0000-0xBFFFF	PCI bus
0xA0000-0xBFFFF	VgaSave
0xC0000-0xDFFFF	PCI bus
0x80000000-0xFFFFFFFF	PCI bus
0x68000000-0x7FFFFFFF	Motherboard resources
0xC0000000-0xFFFFFFFF	Video Controller (VGA Compatible)
0xFEB00000-0xFEB3FFFF	Video Controller (VGA Compatible)
0xFEB44000-0xFEB47FFF	Microsoft UAA Bus Driver for High Definition Audio
0xFE000000-0xFEFFFFFF	PCI standard PCI-to-PCI bridge
0xFE900000-0xFE9FFFFFF	PCI standard PCI-to-PCI bridge
0xFE800000-0xFE8FFFFFF	PCI standard PCI-to-PCI bridge
0xFE800000-0xFE8FFFFFF	Ethernet Controller
0xD0000000-0xD00FFFFFF	PCI standard PCI-to-PCI bridge
0xD0000000-0xD00FFFFFF	Ethernet Controller
0xFEB4F000-0xFEB4F3FF	Standard Dual Channel PCI IDE Controller
0xFEB4E000-0xFEB4EFFF	Standard OpenHCD USB Host Controller
0xFEB4D000-0xFEB4D0FF	Standard Enhanced PCI to USB Host Controller
0xFEB4C000-0xFEB4CFFF	Standard OpenHCD USB Host Controller
0xFEB4B000-0xFEB4B0FF	Standard Enhanced PCI to USB Host Controller
0xFEB40000-0xFEB43FFF	Microsoft UAA Bus Driver for High Definition Audio
0xFEC00000-0xFEC00FFF	Motherboard resources
0xFEE00000-0xFEE00FFF	Motherboard resources
0xFED80000-0xFED8FFFF	Motherboard resources
0xFED61000-0xFED70FFF	Motherboard resources
0xFEC10000-0xFEC10FFF	Motherboard resources
0xFED00000-0xFED00FFF	Motherboard resources

0xFED00000-0xFED00FFF	High precision event timer
0xFFC00000-0xFFFFFFFF	Motherboard resources
0xFEB4A000-0xFEB4AFFF	Standard OpenHCD USB Host Controller
0xFEB49000-0xFEB49FFF	Standard OpenHCD USB Host Controller
0xFEB48000-0xFEB480FF	Standard Enhanced PCI to USB Host Controller
0xE0000000-0xFFFFFFFF	System board
FED45000-FED8FFFF	Motherboard resources
FED90000-FED93FFF	Motherboard resources
FEE00000-FEEFFFFFF	Motherboard resources
FF000000-FFFFFFFF	Intel(R) 82802 Firmware Hub Device
FF000000-FFFFFFFF	Motherboard resources

Appendix C: Interrupt Request Lines (IRQ)

Peripheral devices use interrupt request lines to notify CPU for the service required. The following table shows the IRQ used by the devices on board.

Level	Function
IRQ 9	Microsoft ACPI-Compliant System
IRQ 11	Video Controller (VGA Compatible)
IRQ 19	Microsoft UAA Bus Driver for High Definition Audio
IRQ 19	PCI standard PCI-to-PCI bridge
IRQ 19	Standard Dual Channel PCI IDE Controller
IRQ 16	PCI standard PCI-to-PCI bridge
IRQ 16	Microsoft UAA Bus Driver for High Definition Audio
IRQ 17	PCI standard PCI-to-PCI bridge
IRQ 17	Standard Dual Channel PCI IDE Controller
IRQ 17	Standard Enhanced PCI to USB Host Controller
IRQ 17	Standard Enhanced PCI to USB Host Controller
IRQ 17	Standard Enhanced PCI to USB Host Controller
IRQ 18	PCI standard PCI-to-PCI bridge
IRQ 18	Standard Dual Channel PCI IDE Controller
IRQ 18	Standard OpenHCD USB Host Controller

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IRQ 18	Standard OpenHCD USB Host Controller
IRQ 18	Standard OpenHCD USB Host Controller
IRQ 18	Standard OpenHCD USB Host Controller
IRQ 10	Ethernet Controller
IRQ 7	Communications Port (COM3)
IRQ 7	Communications Port (COM4)
IRQ 1	Standard 101/102-Key or Microsoft Natural PS/2 Keyboard
IRQ 12	Microsoft PS/2 Mouse
IRQ 4	Communications Port (COM1)
IRQ 3	Communications Port (COM2)
IRQ 0	System timer
IRQ 8	System CMOS/real time clock
IRQ 13	Numeric data processor

Appendix D: Watchdog Timer (WDT) Setting

WDT is widely used for industry application to monitor the activity of CPU. Application software depends on its requirement to trigger WDT with adequate timer setting. Before WDT time out, the functional normal system will reload the WDT. The WDT never time out for a normal system. Then, WDT will time out and reset the system automatically to avoid abnormal operation.

This board supports 255 levels watchdog timer by software programming. Below are the source codes written in C, please take them for WDT application examples.

C language Code

```
/*----- Include Header Area -----*/
#include "math.h"
#include "stdio.h"
#include "dos.h"

/*----- routing, sub-routing -----*/

void main()
{
/*----- index port 0x2e -----*/
    outportb(0x2e, 0x87);           /* initial IO port */
    outportb(0x2e, 0x87);           /* twice, */

    outportb(0x2e, 0x07);          /* point to logical device */
    outportb(0x2e+1, 0x07);         /* * select logical device 7 */
    outportb(0x2e, 0xf5);          /* * select offset f5h */
    outportb(0x2e+1, 0x40);         /* * set bit5 = 1 to clear bit5 */
    outportb(0x2e, 0xf0);          /* * select offset f0h */
    outportb(0x2e+1, 0x81);         /* * set bit7 =1 to enable WDTRST# */
    outportb(0x2e, 0xf6);          /* * select offset f6h */
    outportb(0x2e+1, 0x05);         /* * update offset f6h to 0ah :10sec */
    outportb(0x2e, 0xf5);          /* * select offset f5h */
    outportb(0x2e+1, 0x20);         /* * set bit5 = 1 enable watch dog time */

    outportb(0x2e, 0xAA);          /* stop program F71869E, Exit */
}
```

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