EmETXe-a10M3

COM Express® Basic
Type 6 CPU Module

User's Manual

Version 1.1

2021.06

Revision History

Version	Date	Description
1.0	2020.04	Initial release
1.1	2021.06	Revise optional accessory items

Copyright Notice

The information in this document is subject to change without prior notice in order to improve the reliability, design and function. It does not represent a commitment on the part of the manufacturer.

Under no circumstances will the manufacturer be liable for any direct, indirect, special, incidental, or consequential damages arising from the use or inability to use the product or documentation, even if advised of the possibility of such damages.

Declaration of Conformity

CE

The CE symbol on your product indicates that it is in compliance with the directives of the Union European (EU). A Certificate of Compliance is available by contacting Technical Support.

This product has passed the CE test for environmental specifications when shielded cables are used for external wiring. We recommend the use of shielded cables. This kind of cable is available from ARBOR. Please contact your local supplier for ordering information.

This product has passed the CE test for environmental specifications. Test conditions for passing included the equipment being operated within an industrial enclosure. In order to protect the product from being damaged by ESD (Electrostatic Discharge) and EMI leakage, we strongly recommend the use of CE-compliant industrial enclosure products.

> Warning
>
> This is a class A product. In a domestic environment this product may cause radio interference in which case the user may be required to take adequate measures.

FCC Class B

This device complies with Part 15 of the FCC Rules. Operation is subject to the following two conditions:

(1)This device may not cause harmful interference, and

(2)This device must accept any interference received, including interference that may cause undesired operation.

NOTE:

This equipment has been tested and found to comply with the limits for a Class A digital device, pursuant to Part 15 of the FCC Rules. These limits are designed to provide reasonable protection against harmful interference when the equipment is operated in a commercial environment. This equipment generates, uses, and can radiate radio frequency energy and, if not installed and used in accordance with the instruction manual, may cause harmful interference to radio communications. Operation of this equipment in a residential area is likely to cause harmful interference in which case the user will be required to correct the interference at his own expense.

RoHS

ARBOR Technology Corp. certifies that all components in its products are in compliance and conform to the European Union's Restriction of Use of Hazardous Substances in Electrical and Electronic Equipment (RoHS) Directive 2002/95/EC.

The above mentioned directive was published on 2/13/2003. The main purpose of the directive is to prohibit the use of lead, mercury, cadmium, hexavalent chromium, polybrominated biphenyls (PBB), and polybrominated diphenyl ethers (PBDE) in electrical and electronic products. Member states of the EU are to enforce by 7/1/2006.

ARBOR Technology Corp. hereby states that the listed products do not contain unintentional additions of lead, mercury, hex chrome, PBB or PBDB that exceed a maximum concentration value of 0.1% by weight or for cadmium exceed 0.01% by weight, per homogenous material. Homogenous material is defined as a substance or mixture of substances with uniform composition (such as solders, resins, plating, etc.). Lead-free solder is used for all terminations (Sn(96-96.5%), Ag(3.0-3.5%) and Cu(0.5%)).

SVHC / REACH

To minimize the environmental impact and take more responsibility to the earth we live, Arbor hereby confirms all products comply with the restriction of SVHC (Substances of Very High Concern) in (EC) 1907/2006 (REACH --Registration, Evaluation, Authorization, and Restriction of Chemicals) regulated by the European Union.

All substances listed in SVHC < 0.1 % by weight (1000 ppm)

Warning

Single Board Computers and their components contain very delicate Integrated Circuits (IC). To protect the Single Board Computer and its components against damage from static electricity, you should always follow the following precautions when handling it :

1. Disconnect your Single Board Computer from the power source when you want to work on the inside.

2. Hold the board by the edges and try not to touch the IC chips, leads or circuitry.

3. Use a grounded wrist strap when handling computer components.

4. Place components on a grounded antistatic pad or on the bag that comes with the Single Board Computer, whenever components are separated from the system.

Replacing the Lithium Battery

Incorrect replacement of the lithium battery may lead to a risk of explosion.

The lithium battery must be replaced with an identical battery or a battery type recommended by the manufacturer.

Do not throw lithium batteries into the trash-can. It must be disposed of in accordance with local regulations concerning special waste.

Technical Support

If you have any technical difficulties, please contact our website at:

https://www.arbor-technology.com

Warranty

This product is warranted to be in good working order for a period of two years from the date of purchase. Should this product fail to be in good working order at any time during this period, we will, at our option, replace or repair it at no additional charge except as set forth in the following terms. This warranty does not apply to products damaged by misuse, modifications, accident or disaster.

Vendor assumes no liability for any damages, lost profits, lost savings or any other incidental or consequential damage resulting from the use, misuse of, or inability to use this product. Vendor will not be liable for any claim made by any other related party.

Vendors disclaim all other warranties, either expressed or implied, including but not limited to implied warranties of merchantability and fitness for a particular purpose, with respect to the hardware, the accompanying product's manual(s) and written materials, and any accompanying hardware. This limited warranty gives you specific legal rights.

Return authorization must be obtained from the vendor before returned merchandise will be accepted. Authorization can be obtained by calling or faxing the vendor and requesting a Return Merchandise Authorization (RMA) number. Returned goods should always be accompanied by a clear problem description.

Chapter 1

Introduction

1.1 The Product

The EmETXe-a10M3 is a space-conscious CPU board of 125 mm x 95 mm to take up only small footprint in your system. By the architecture of Type 6, the board has two high-performance connectors to promise stable data passing rate. The soldered onboard AMD Ryzen V1000 processor, along with integrated AMD Vega Core graphics chipset bring LVDS, and DDI solution for most monitors or LCD video panels.

For system configuration, the board is supported by AMI UEFI BIOS. EmETXe-a10M3 is an ideal choice for some demanding industrial control and data communications by its significant processing performance, low power consumption and these features:

- Soldered onboard AMD V1605B/V1756B/B1807B APU Processor
- Integrated Gigabit Ethernet
- Dual Channels 24-bit LVDS or 1 x DP port, 3 x DDI ports
- Support 3 independent displays

1.2 About This Manual

This user's manual provides general information and installation instructions about the product. This user's manual is intended for experienced users and integrators with hardware knowledge of personal computers. If you are not sure about any description in this booklet. Please consult your vendor before further handling.

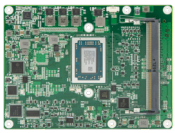
1.3 Specifications

System	
CPU	Soldered onboard AMD Ryzen V1000 V1605B 2.0GHz(Base)/ 3.6GHz (Turbo) or V1756B 3.25GHz(Base)/ 3.6GHz (Turbo) or V1807B 3.25GHz(Base)/ 3.8GHz (Turbo) processor
Memory	2 x DDR4 ECC SO-DIMM sockets, supporting up to 32GB SDRAM
BIOS	AMI UEFI BIOS
Watchdog Timer	1~255 levels reset
I/O	
USB Port	12 x USB ports: - 8 x USB 2.0 ports - 4 x USB 3.1 ports
Serial Port	2 x UART ports (RX/TX only)
Expansion Bus	8 x PCIe x1 lanes 1 x PCIe x8 lane, LPC, SPI
DIO	8-bit Digital Input/Output
Storage	2 x Serial ATA ports with 600MB/s HDD transfer rate
Ethernet Chipset	1 x Intel® i210IT GbE controller
Audio	HD audio link
TPM	Supports TPM 2.0 SLB9665TT
Display	
Graphic Chipset	Integrated Vega Core Graphics controller
Graphic Interface	Dual Channels 24-bit LVDS, with resolution up to 1920 x 1200 @60Hz
	3 x DDI ports

OS support	Windows 10 64-bit, Linux: Ubuntu
Mechanical & Environmental	
Power Requirement	8.5V~28V 5% wide range voltage input
Power Consumption	2.39A@12V (V1605B typical)
Operating Temp.	-20 ~ 70°C (-4 ~ 158°F)
Operating Humidity	10 ~ 95% @ 70ºC (non-condensing)
Dimension (L x W)	125 x 95 mm (4.9” x 3.7”)

1.4 Inside the Package

Before you begin installing your single board, please make sure that the following materials have been shipped:



1 x EmETXe-a10M3 COM Express CPU Module

1 x Quick Installation Guide

If any of the above items is damaged or missing, contact your vendor immediately.

1.5 Ordering Information

EmETXe-a10M3-V1605B	AMD Ryzen Embedded V1000 V1605B COM Express® Basic Type 6 CPU Module
EmETXe-a10M3-V1756B	AMD Ryzen Embedded V1000 V1756B COM Express® Basic Type 6 CPU Module
EmETXe-a10M3-V1807B	AMD Ryzen Embedded V1000 V1807B COM Express® Basic Type 6 CPU Module

1.5.1 Optional Accessories

HS-10M3-C1	Heat sink with Fan, PAD (95x95x51mm)
PBE-1705-F1	COM Express® Type 6 evaluation carrier board with SIO F71869ED module in ATX form factor
CBK-03-1705-00	Cable kit 1 x SATA cable 2 x COM Flat cables

1.6 Driver(7.2A) Installation

To install the drivers, please visit our website at **www.arbor.technology.com** and download the driver pack from the product page.

Driver	Path
Audio	\EmETXe-a10R0\Audio\Win10_Win8.1_Win8_Win7_WHQLx64
Chipset	\EmETXe-a10R0\SOC
LAN	\EmETXe-a10R0\LAN

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Chapter 2

Board Overview

2.1 What Is "COM Express®"?

With more and more demands on small and embedded industrial boards, a multi-functional COM (Computer-on-Module) surfaces as a great solution.

COM Express® supports seven pin-out types applying to Basic and Extended form factors:

Module Type 1 and 10 support single connector with two rows (220 pins).

Module Type 2, 3, 4, 5 and 6 support two connectors with four rows (440 pins).

EmETXe-a10M3 is a Type-6 module.

Difference between Standard Type 6 and EmETXe-a10M3 is listed as below:

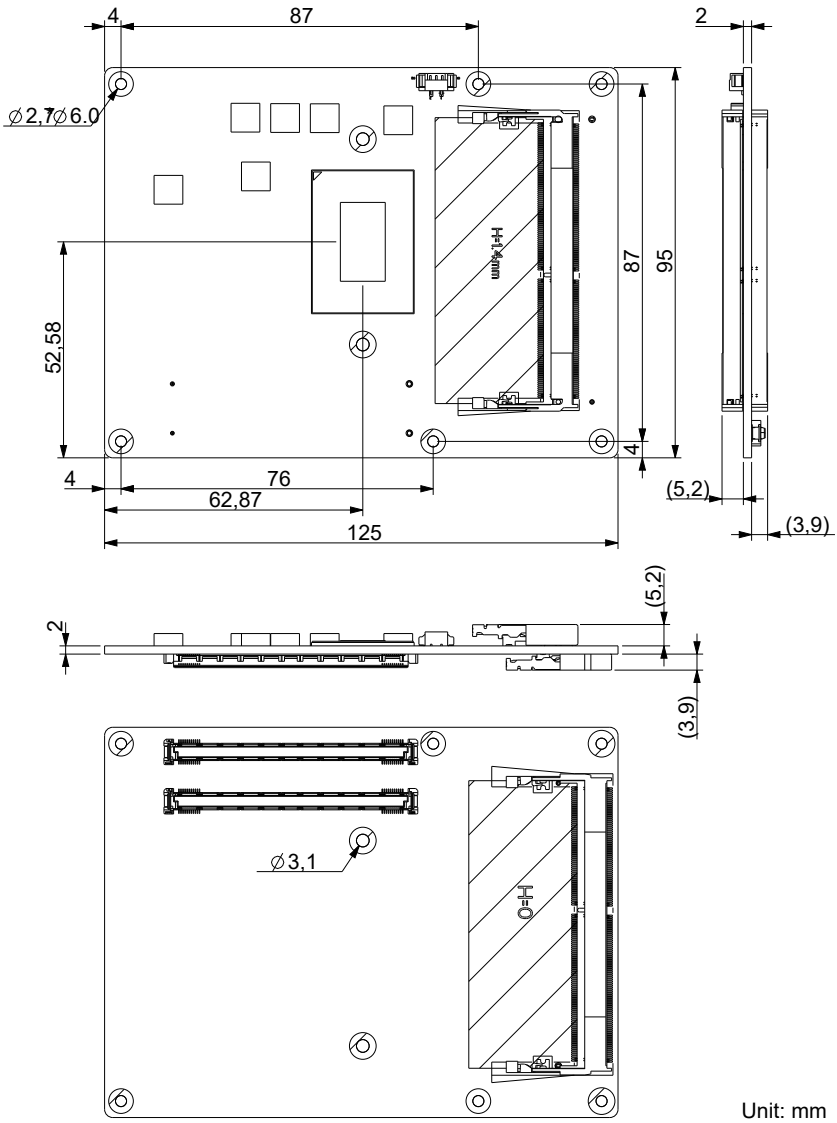
Module Type	Standard Type 6	EmETXe-a10M3
Connectors	2	2
Connector Rows	A, B, C, D	A, B, C, D
PCIe Lanes (Max)	24	24
LAN (Max)	1	1
Serial Ports (Max)	2	2
Digital Display I/F (Max)	3	3
USB 3.0 Ports (Max)	4	4

Row AB provides pins for PCI Express, SATA, LVDS, LCD channel, LPC bus, system and power management, VGA, LAN, and power and ground interfaces.

Row CD provides SDVO and legacy PCI signals next to additional PCI Express, LAN and power and ground signals. The COM are targeted at following applications:

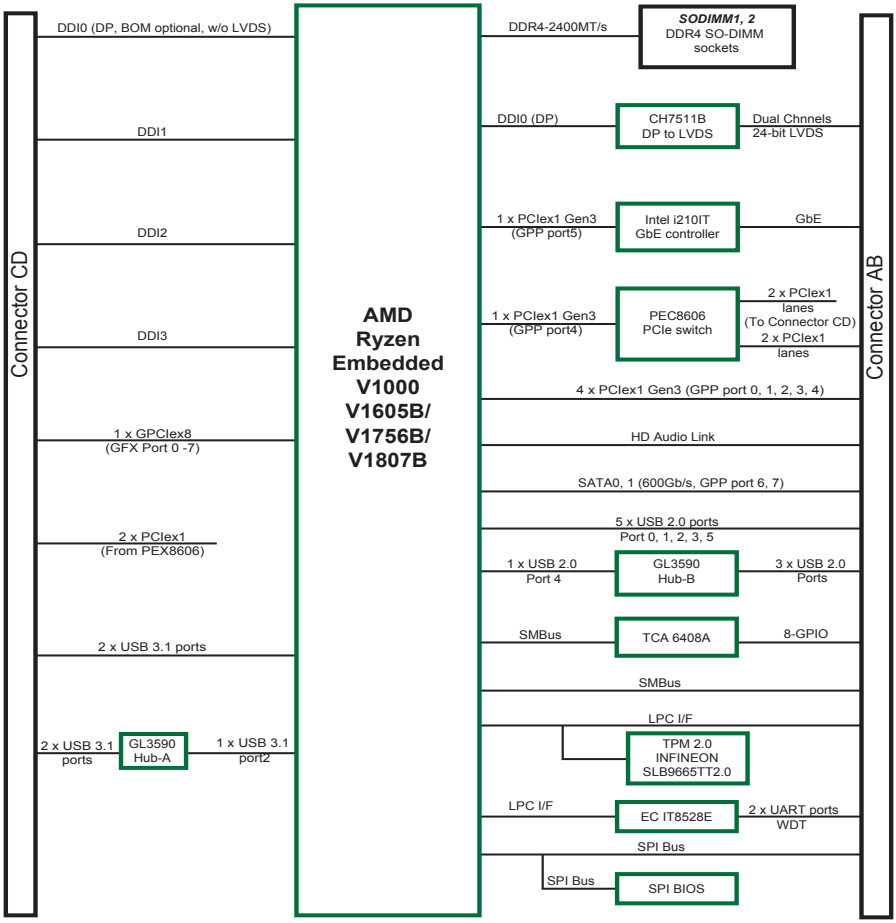
- Retail & Advertising
- Medical
- Test & Measurement
- Gaming & Entertainment
- Industrial & Automation
- Military & Government
- Security

2.2 Board Dimensions



Unit: mm

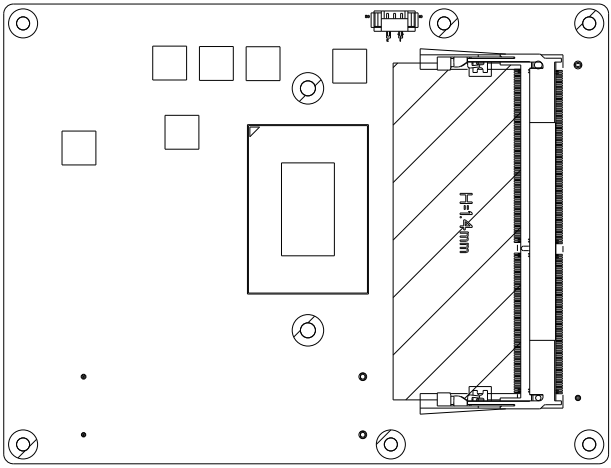
2.3 Block Diagram



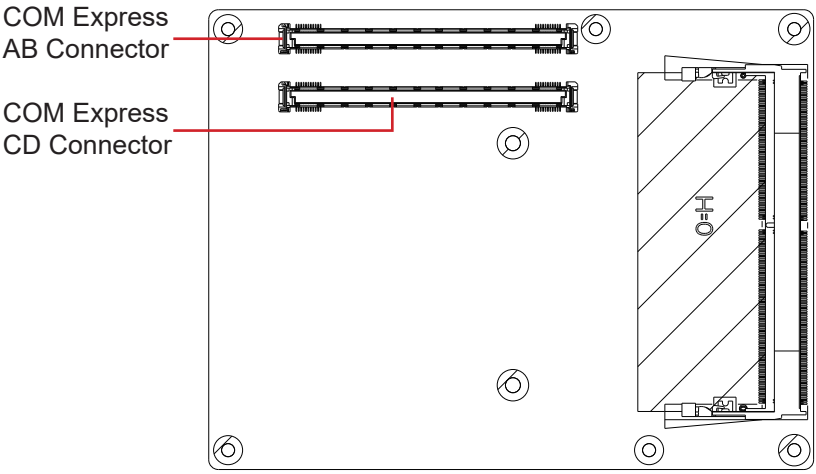
2.4 Connector Pin Definition

Being a most commonly-used Type 6, the EmETXe-a10M3 features two board-to-board connectors on bottom side.

Top Side



Bottom Side



COM Express AB Connector (bottom side)

B1	GND(FIXED)	GND(FIXED)	A1
B2	GBE0_ACT#	GBE0_MDI3-	A2
B3	LPC_FRAME#	GBE0_MDI3+	A3
B4	LPC_AD0	GBE0_LINK100#	A4
B5	LPC_AD1	GBE0_LINK1000#	A5
B6	LPC_AD2	GBE0_MDI2-	A6
B7	LPC_AD3	GBE0_MDI2+	A7
B8	LPC_DRQ0#	N/C	A8
B9	LPC_DRQ1#	GBE0_MDI1-	A9
B10	LPC_CLK	GBE0_MDI1+	A10
B11	GND(FIXED)	GND(FIXED)	A11
B12	PWRBTN#	GBE0_MDI0-	A12
B13	SMB_CK	GBE0_MDI0+	A13
B14	SMB_DAT	N/C	A14
B15	SMB_ALERT#	SUS_S3#	A15
B16	SATA1_TX+	SATA0_TX+	A16
B17	SATA1_TX-	SATA0_TX-	A17
B18	SUS_STAT#	SUS_S4#	A18
B19	SATA1_RX+	SATA0_RX+	A19
B20	SATA1_RX-	SATA0_RX-	A20
B21	GND(FIXED)	GND(FIXED)	A21
B22	N/C	N/C	A22
B23	N/C	N/C	A23
B24	PWR_OK	SUS_S5#	A24
B25	N/C	N/C	A25
B26	N/C	N/C-	A26
B27	WDT	BATLOW#	A27
B28	AD/HAD_SDIN2	(S)ATA_ACT#	A28
B29	AD/HAD_SDIN1	AC/HAD_SYNC	A29
B30	AD/HAD_SDIN0	AC/HAD_RST#	A30
B31	GND(FIXED)	GND(FIXED)	A31
B32	SPKR	AC/HAD_BITCLK	A32
B33	I2C_CK	AC/HAD_SDOUT	A33
B34	I2C_DAT	BIOS_DIS0#	A34
B35	THRM#	THRMTRIP#	A35
B36	USB7-	USB6-	A36
B37	USB7+	USB6+	A37
B38	USB_4_5_OC#	USB_6_7_OC#	A38
B39	USB5-	USB4-	A39
B40	USB5+	USB4+	A40
B41	GND(FIXED)	GND(FIXED)	A41
B42	USB3-	USB2-	A42
B43	USB3+	USB2+	A43
B44	USB_0_1_OC#	USB_2_3_OC#	A44
B45	USB1-	USB0-	A45
B46	USB1+	USB0+	A46
B47	EXCD1_PERST#	VCC_RTC	A47
B48	EXCD1_CPPE#	EXCD0_PERST#	A48
B49	SYS_RESET#	EXCD0_CPPE#	A49
B50	CB_RESET#	LPC_SERIRQ	A50
B51	GND(FIXED)	GND(FIXED)	A51
B52	PCIE_RX5+	PCIE_TX5+	A52
B53	PCIE_RX5-	PCIE_TX5-	A53
B54	GPO1	GPI0	A54
B55	PCIE_RX4+	PCIE_TX4+	A55

B56	PCIE_RX4-	PCIE_TX4-	A56
B57	GND	GND	A57
B58	PCIE_RX3+	PCIE_TX3+	A58
B59	PCIE_RX3-	PCIE_TX3-	A59
B60	GND(FIXED)	GND(FIXED)	A60
B61	PCIE_RX2+	PCIE_TX2+	A61
B62	PCIE_RX2-	PCIE_TX2-	A62
B63	GPO3	GPI1	A63
B64	PCIE_RX1+	PCIE_TX1+	A64
B65	PCIE_RX1-	PCIE_TX1-	A65
B66	WAKE0#	GND	A66
B67	WAKE1#	GPI2	A67
B68	PCIE_RX0+	PCIE_TX0+	A68
B69	PCIE_RX0-	PCIE_TX0-	A69
B70	GND(FIXED)	GND(FIXED)	A70
B71	LVDS_B0+	LVDS_A0+	A71
B72	LVDS_B0-	LVDS_A0-	A72
B73	LVDS_B1+	LVDS_A1+	A73
B74	LVDS_B1-	LVDS_A1-	A74
B75	LVDS_B2+	LVDS_A2+	A75
B76	LVDS_B2-	LVDS_A2-	A76
B77	LVDS_B3+	LVDS_VDD_EN	A77
B78	LVDS_B3-	LVDS_A3+	A78
B79	LVDS_BKLT_EN	LVDS_A3-	A79
B80	GND(FIXED)	GND(FIXED)	A80
B81	LVDS_B_CK+	LVDS_A_CK+	A81
B82	LVDS_B_CK-	LVDS_A_CK-	A82
B83	LVDS_BKLT_CTRL	LVDS_I2C_CK	A83
B84	VCC_5V _SBY	LVDS_I2C_DAT	A84
B85	VCC_5V _SBY	GPI3	A85
B86	VCC_5V _SBY	RSVD	A86
B87	VCC_5V _SBY	RSVD	A87
B88	BIOS_DIS1#	PCIE_CLK_REF+	A88
B89	N/C	PCIE_CLK_REF-	A89
B90	GND(FIXED)	GND(FIXED)	A90
B91	N/C	SPI_POWER	A91
B92	N/C	SPI_MISO	A92
B93	N/C	GPO0	A93
B94	N/C	SPI_CLK	A94
B95	N/C	SPI_MOSI	A95
B96	N/C	TPM_PP	A96
B97	SPI_CS#	N/C	A97
B98	N/C	SER0_TX	A98
B99	N/C	SER0_RX	A99
B100	GND(FIXED)	GND(FIXED)	A100
B101	FAN_PWNOUT	SER1_TX	A101
B102	FAN_TACHIN	SER1_RX	A102
B103	SLEEP#	LID#	A103
B104	VCC_12V	VCC_12V	A104
B105	VCC_12V	VCC_12V	A105
B106	VCC_12V	VCC_12V	A106
B107	VCC_12V	VCC_12V	A107
B108	VCC_12V	VCC_12V	A108
B109	VCC_12V	VCC_12V	A109
B110	GND(FIXED)	GND(FIXED)	A110

COM Express CD Connector (bottom side)

D1	GND(FIXED)	GND(FIXED)	C1
D2	GND	GND	C2
D3	USB_SSTX0-	USB_SSRX0-	C3
D4	USB_SSTX0+	USB_SSRX0+	C4
D5	GND	GND	C5
D6	USB_SSTX1-	USB_SSRX1-	C6
D7	USB_SSTX1+	USB_SSRX1+	C7
D8	GND	GND	C8
D9	USB_SSTX2-	USB_SSRX2-	C9
D10	USB_SSTX2+	USB_SSRX2+	C10
D11	GND(FIXED)	GND(FIXED)	C11
D12	USB_SSTX3-	USB_SSRX3-	C12
D13	USB_SSTX3+	USB_SSRX3+	C13
D14	GND	GND	C14
D15	DDI1_CTRLCLK_AUX+	N/C	C15
D16	DDI1_CTRLCLK_AUX-	N/C	C16
D17	RSVD	RSVD	C17
D18	RSVD	RSVD	C18
D19	PCIE_TX6+	PCIE_RX6+	C19
D20	PCIE_TX6-	PCIE_RX6-	C20
D21	GND(FIXED)	GND(FIXED)	C21
D22	PCIE_TX7+	PCIE_RX7+	C22
D23	PCIE_TX7-	PCIE_RX7-	C23
D24	RSVD	DDI1_HPD	C24
D25	RSVD	N/C	C25
D26	DDI1_PAIR0+	N/C	C26
D27	DDI1_PAIR0-	RSVD	C27
D28	RSVD	RSVD	C28
D29	DDI1_PAIR1+	N/C	C29
D30	DDI1_PAIR1-	N/C	C30
D31	GND(FIXED)	GND(FIXED)	C31
D32	DDI1_PAIR2+	DDI2_CTRLCLK_AUX+	C32
D33	DDI1_PAIR2-	DDI2_CTRLCLK_AUX-	C33
D34	DDI1_DDC_AUX_SEL	DDI2_DDC_AUX_SEL	C34
D35	RSVD	RSVD	C35
D36	DDI1_PAIR3+	DDI3_CTRLCLK_AUX+	C36
D37	DDI1_PAIR3-	DDI3_CTRLCLK_AUX-	C37
D38	RSVD	DDI3_DDC_AUX_SEL	C38
D39	DDI2_PAIR0+	DDI3_PAIR0+	C39
D40	DDI2_PAIR0-	DDI3_PAIR0-	C40
D41	GND(FIXED)	GND(FIXED)	C41
D42	DDI2_PAIR1+	DDI3_PAIR1+	C42
D43	DDI2_PAIR1-	DDI3_PAIR1-	C43
D44	DDI2_HPD	DDI3_HPD	C44
D45	RSVD	RSVD	C45
D46	DDI2_PAIR2+	DDI3_PAIR2+	C46
D47	DDI2_PAIR2-	DDI3_PAIR2-	C47
D48	RSVD	RSVD	C48
D49	DDI2_PAIR3+	DDI3_PAIR3+	C49
D50	DDI2_PAIR3-	DDI3_PAIR3-	C50
D51	GND(FIXED)	GND(FIXED)	C51
D52	PEG_TX0+	PEG_RX0+	C52
D53	PEG_TX0-	PEG_RX0-	C53
D54	PEG_LANE_RV#	TYPE0#	C54
D55	PEG_TX1+	PEG_RX1+	C55

D56	PEG_TX1-	PEG_RX1-	C56
D57	TYPE2#	TYPE1#	C57
D58	PEG_TX2+	PEG_RX2+	C58
D59	PEG_TX2-	PEG_RX2-	C59
D60	GND(FIXED)	GND(FIXED)	C60
D61	PCIE_TX3+	PCIE_RX3+	C61
D62	PCIE_TX3-	PCIE_RX3-	C62
D63	RSVD	RSVD	C63
D64	RSVD	RSVD	C64
D65	PCIE_TX4+	PCIE_RX4+	C65
D66	PCIE_TX4-	PCIE_RX4-	C66
D67	RSVD	RSVD	C67
D68	PCIE_TX5+	PCIE_RX5+	C68
D69	PCIE_TX5-	PCIE_RX5-	C69
D70	GND(FIXED)	GND(FIXED)	C70
D71	PCIE_TX6+	PCIE_RX6+	C71
D72	PCIE_TX6-	PCIE_RX6-	C72
D73	GND	GND	C73
D74	PCIE_TX7+	PCIE_RX7+	C74
D75	PCIE_TX7-	PCIE_RX7-	C75
D76	GND	GND	C76
D77	RSVD	RSVD	C77
D78	PCIE_TX8+	N/C	C78
D79	PCIE_TX8-	N/C	C79
D80	GND(FIXED)	GND(FIXED)	C80
D81	PCIE_TX9+	N/C	C81
D82	PCIE_TX9-	N/C	C82
D83	RSVD	RSVD	C83
D84	GND	GND	C84
D85	N/C	N/C	C85
D86	N/C	N/C	C86
D87	GND	GND	C87
D88	N/C	N/C	C88
D89	N/C	N/C	C89
D90	GND(FIXED)	GND(FIXED)	C90
D91	PCIE_TX12+	N/C	C91
D92	PCIE_TX12-	N/C	C92
D93	GND	GND	C93
D94	PCIE_TX13+	N/C	C94
D95	PCIE_TX13-	N/C	C95
D96	GND	GND	C96
D97	RSVD	RSVD	C97
D98	PCIE_TX14+	N/C	C98
D99	PCIE_TX14-	N/C	C99
D100	GND(FIXED)	GND(FIXED)	C100
D101	PCIE_TX15+	N/C	C101
D102	PCIE_TX15-	N/C	C102
D103	GND	GND	C103
D104	VCC_12V	VCC_12V	C104
D105	VCC_12V	VCC_12V	C105
D106	VCC_12V	VCC_12V	C106
D107	VCC_12V	VCC_12V	C107
D108	VCC_12V	VCC_12V	C108
D109	VCC_12V	VCC_12V	C109
D110	GND(FIXED)	GND(FIXED)	C110

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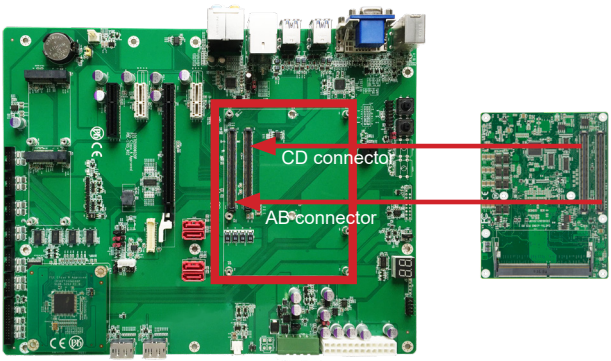
Chapter 3

Installation & Maintenance

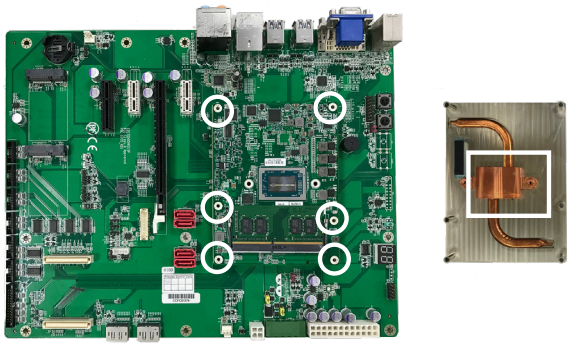
3.1 Installing the CPU Module to Carrier Board

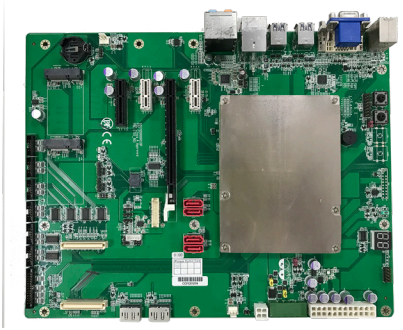
1. Mount the EmETXe-a10M3 into PBE-1705 via COM Express connectors as below; that is, COM Express AB to AB and CD to CD.



2. Install the optional heat spreader or heat sink with fan to the COM module.

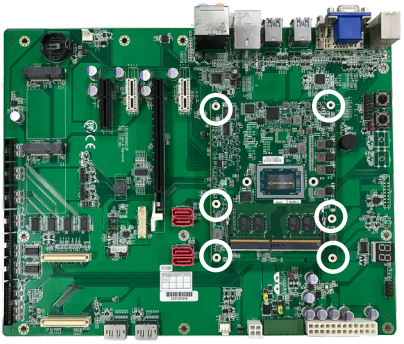
   For heat spreader
   Apply thermal grease to the CPU area on the CPU module. Place the heat spreader over the CPU module and fasten the six screws to secure it in place.

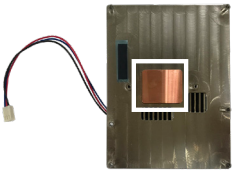




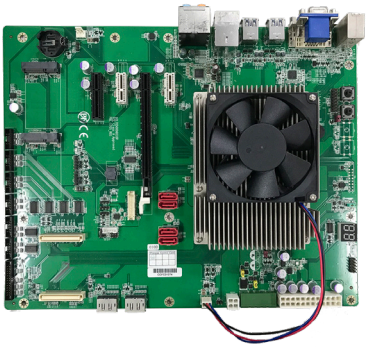
For heat sink with fan

Apply thermal grease to the CPU area on the CPU module. Place the heat sink over the CPU module and fasten the six screws to secure it in place.





Then connect the fan cable to
the fan connector on the carrier board.



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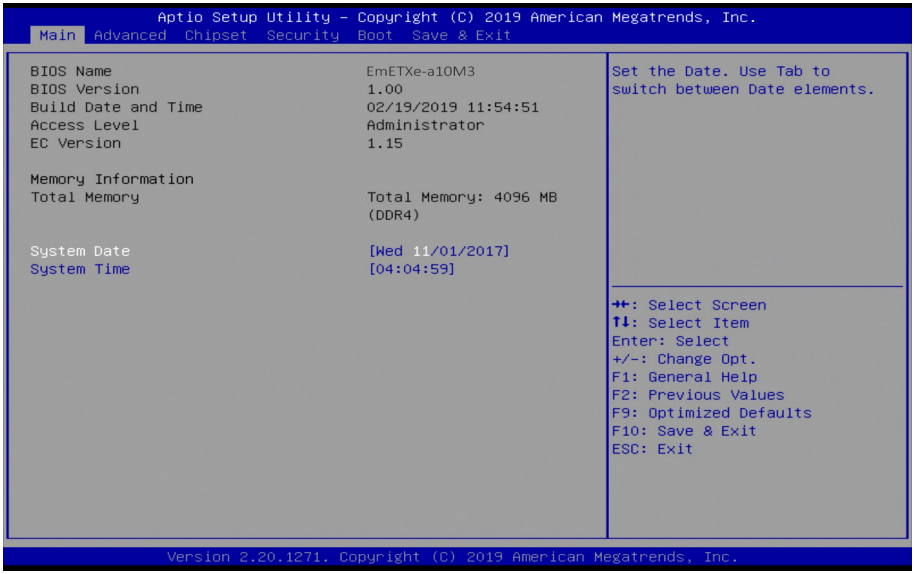
Chapter 4

BIOS

4.1 Main

The Aptio BIOS provides a Setup utility program for specifying the system configurations and settings. The BIOS RAM of the system stores the Setup utility and configurations. When you turn on the computer, the AMI BIOS is immediately activated. To enter the BIOS SETUP UTILITY, press **"Delete"** once the power is turned on. When the computer is shut down, the battery on the motherboard supplies the power for BIOS RAM.

The **Main Setup** screen lists the following information:



Info Item	Description
BIOS Name	Delivers the Project name.
BIOS Version	Delivers the version of BIOS.
Build Date and Time	Delivers the date and time the BIOS Setup utility was made/updated.
Total Memory	Delivers Memory info.
System Date	Sets system date.
System Time	Sets system time.

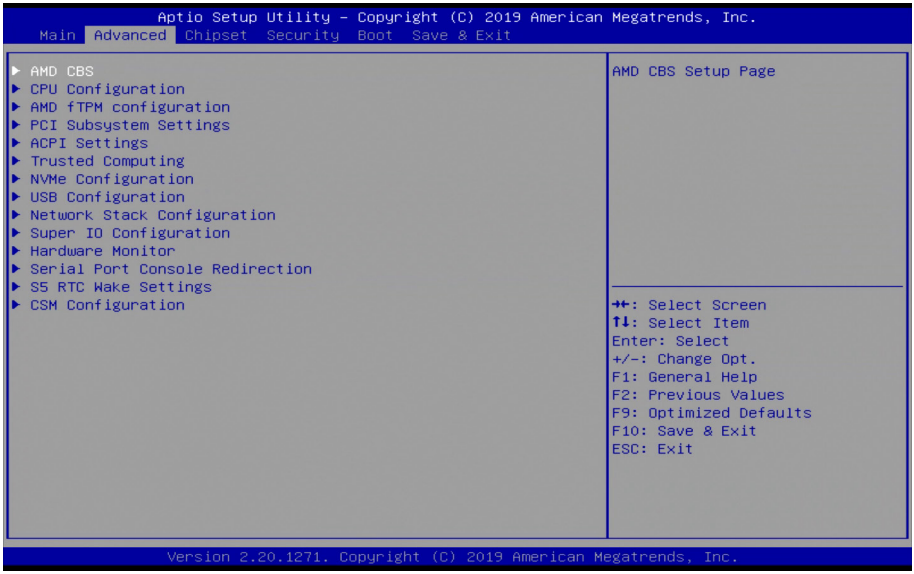
Access Level	Delivers the level by which the BIOS Setup utility is being accessed at the moment.

Key Commands

BIOS Setup Utility is mainly a key-based navigation interface. Please refer to the following key command instructions for navigation process.

Keystroke	Function
◄ ►	Move to highlight a particular configuration screen from the top menu bar / Move to highlight items on the screen
▼ ▲	Move to highlight previous/next item
Enter	Select and access a setup item/field
Esc	On the Main Menu – Quit the setup and not save changes into CMOS (a message screen will display and ask you to select “OK” or “Cancel” for exiting and discarding changes. Use “←” and “→” to select and press “Enter” to confirm) On the Sub Menu – Exit current page and return to main menu
+	Increase the numeric value on a selected setup item / make change
-	Decrease the numeric value on a selected setup item / make change
F1	Activate “General Help” screen
F2	Restore previous values
F9	Use optimized defaults
F10	Save the changes that have been made in the setup and exit. (a message screen will display and ask you to select “OK” or “Cancel” for exiting and saving changes. Use “←” and “→” to select and press “Enter” to confirm)

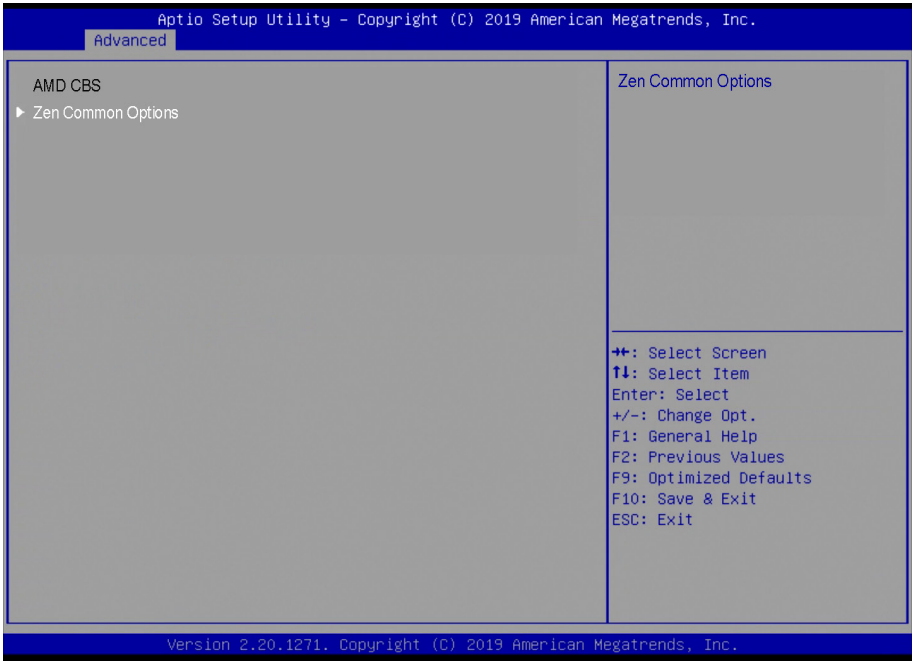
4.2 Advanced



Setting	Description
AMD CBS	See 4.2.1 AMD CBS on page 23
CPU Configuration	See 4.2.2 CPU Configuration on page 24
AMC fTPM Configuration	See 4.2.3 AMD fTPM Configuration on page 25
PCI Subsystem Settings	See 4.2.4 PCI Subsystem Settings on page 26
ACPI Settings	See 4.2.5 ACPI Settings on page 27
Trusted Computing	See 4.2.6 Trusted Computing on page 28
NVMe Configuration	See 4.2.7 NVMe Configuration on page 29
USB Configuration	See 4.2.8 USB Configuration on page 30
Network Stack Configuration	See 4.2.9 Network Stack Configuration on page 32
Super IO Configuration	See 4.2.10 Super IO Configuration on page 33
H/W Monitor	See 4.2.11 H/W Monitor on page 36
Serial Port Redirection	See 4.2.12 Serial Port Redirection on page 37

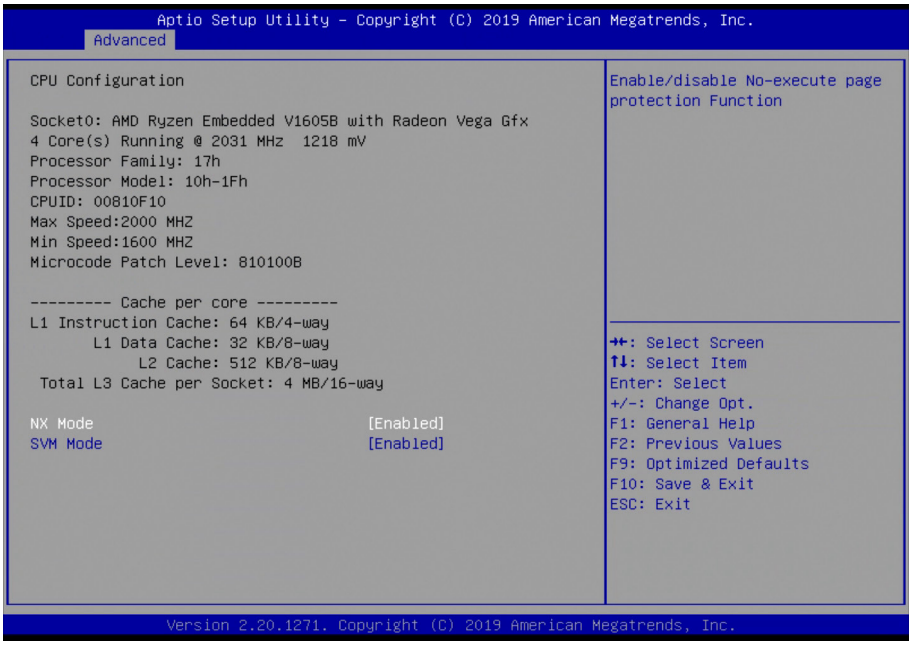
S5 RTC Wake Settings	See 4.2.13 S5 RTC Wake Settings on page 39
CSM Configuration	See 4.2.14 CSM Configuration on page 40

4.2.1 AMD CBS



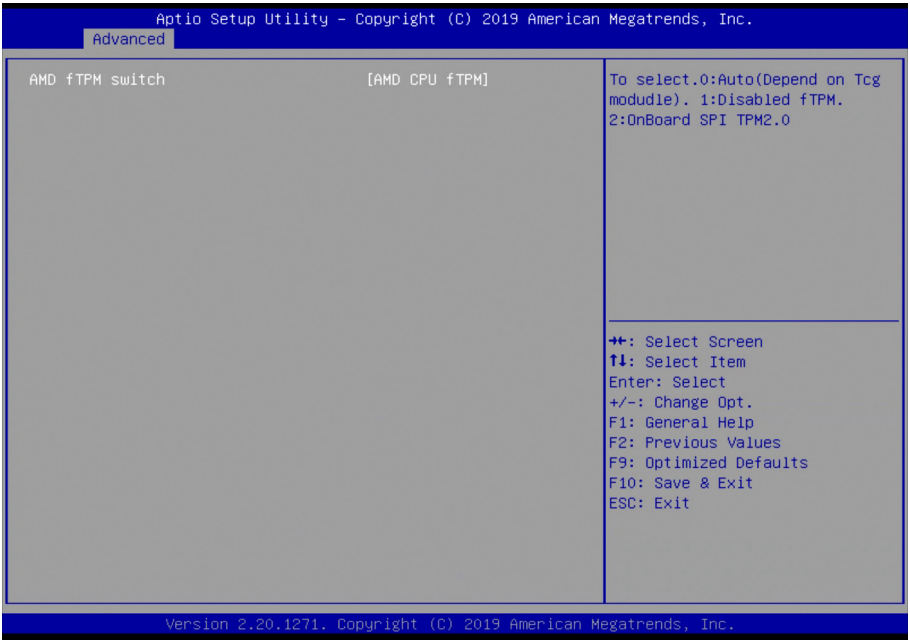
Setting	Description
Zen Common Options	**Gloabl C-Sate Control** **Enables** or **Disables** (default) IO based C-stat generation and DF C-states.

4.2.2 CPU Configuration



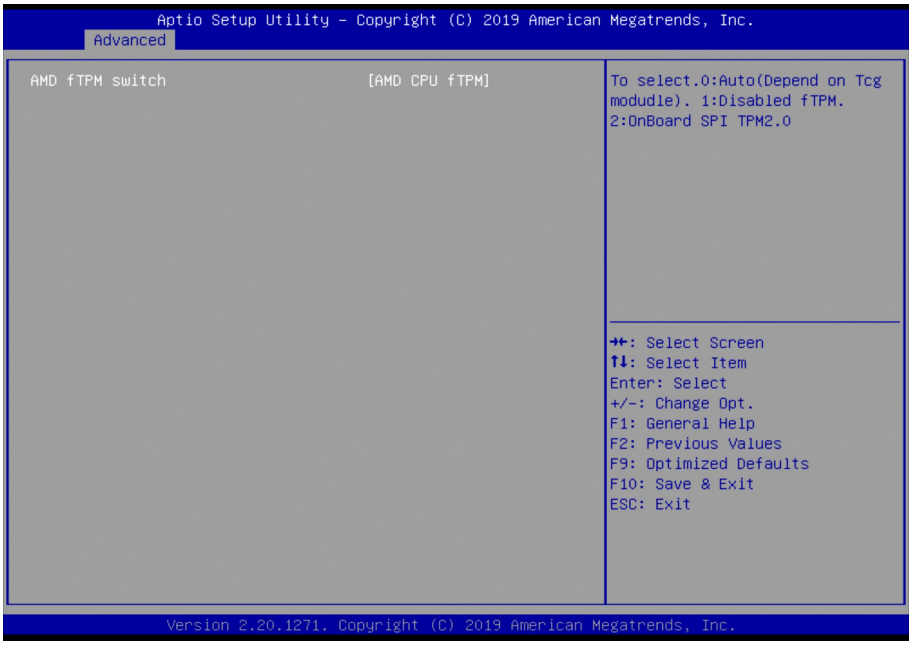
Setting	Description
NX Mode	**Enable** (default) / **Disable** No-execute page protection Function.
SVM Mode	**Enable** (default) / **Disable** CPU Virtualization.

4.2.3 AMD fTPM Configuration



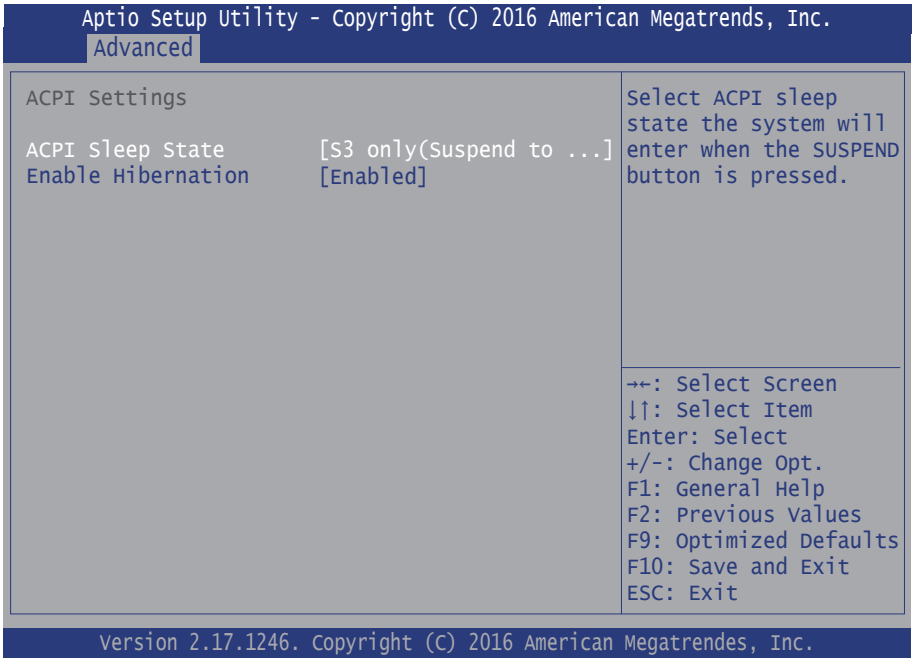
Setting	Description
AMD fTPM Switch	To select AMD fTPM switch. Options: ► **AMD CPU fTPM** (default): Depend on Tcg module) ► **Route to LPC TPM**

4.2.4 PCI Subsystem Settings



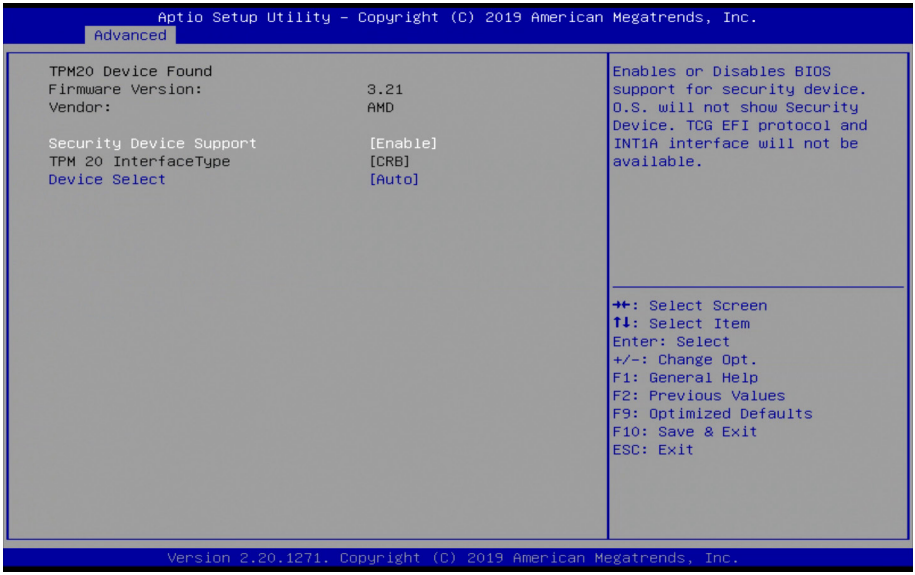
Setting	Description
PCI Latency Timer	Value to be programmed into PCI Latency timer Register. ► Default: **32 PCI Bus Clocks**
PCI-X Latency Timer	Value to be programmed into PCI Latency timer Register. ► Default: **64 PCI Bus Clocks**
Above 4G Decoding	**Enable**/**Disable**(default) 64bit capable Devices to be Decoded in Above 4G Address Space (Only if System Supports 64 bit PCI Decoding).

4.2.5 ACPI Settings



Setting	Description
Enable Hibernation	**Enables** (default) or **Disables** System ability to Hibernate (OS/S4 Sleep State). This option may be not effective with some OS.
ACPI Sleep State	Select ACPI sleep state the system will enter when the SUSPEND button is pressed. ► Options: **Suspend Disabled**, **S3 (Suspend to RAM)** (default)

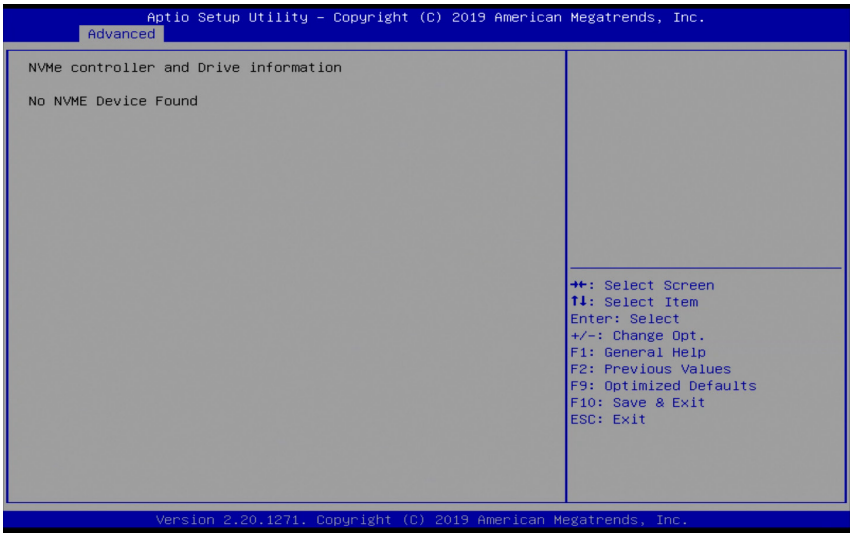
4.2.6 Trusted Computing



Setting	Description
Security Device Support	**Enable** (default) or **Disable** BIOS support for security device. O.S. will not show Security Device. TCG EFI protocol and INT1A interface will not be available.
Device Select	Select the TPM device: Options: **TPM 1.2**, **TPM 2.0** and **Auto** (default) ► TPM 1.2 will restrict supoort to TPM 1.2 devices ► TPM 2.0 will restrict support to TPM 2.0 devices ► Auto will support both with the default set to TPM 2.0 devices if not found., TPM 1.2 device will be enumerated.

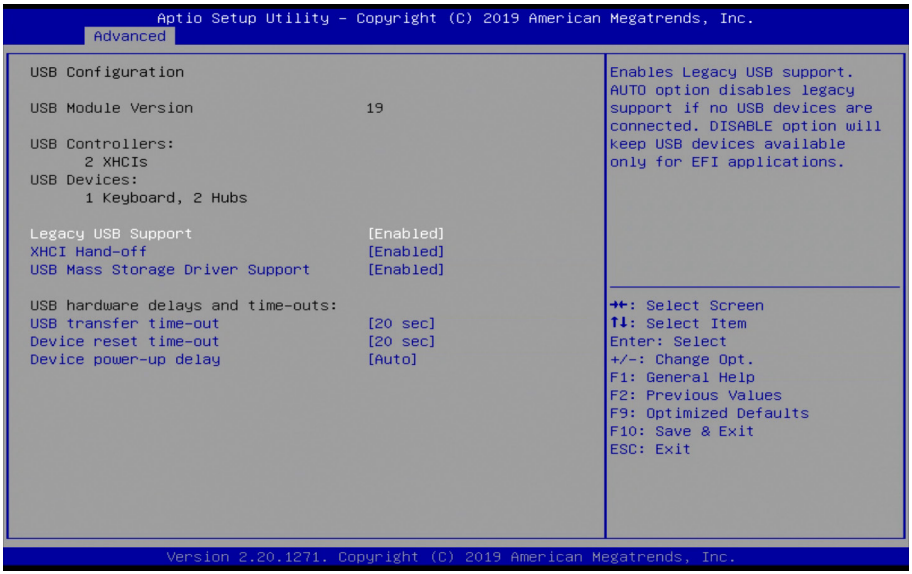
4.2.7 NVMe Configuration

Access this submenu to view the NVMe controller and driver information.



4.2.8 USB Configuration

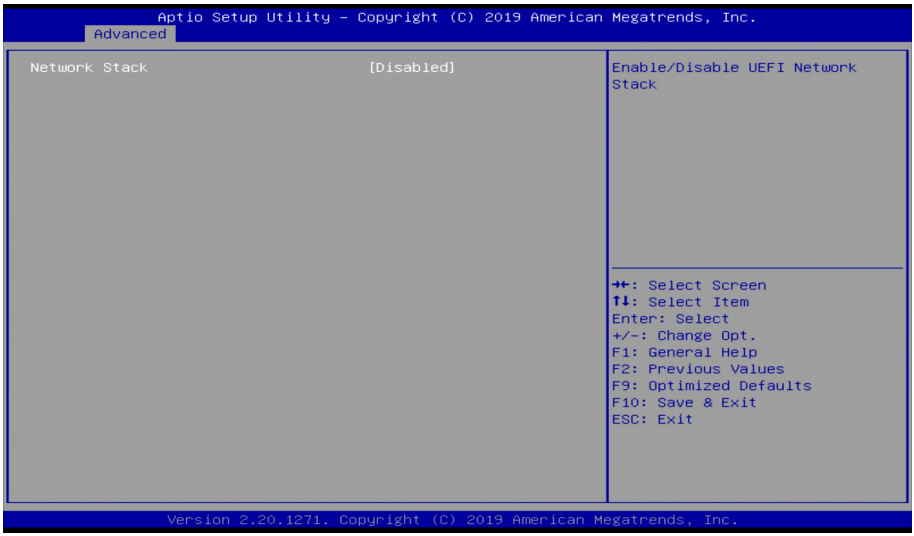
Select this submenu to view the status of the USB ports and configure USB features.



Setting	Description
Legacy USB Support	Sets legacy USB support. ► Options: **Enabled** (default), **Disabled** and **Auto**. **AUTO** option disables legacy support if no USB devices are connected. **Disable** option will keep USB devices available only for EFI applications.
XHCI Hand-off	**Enable** (default) or **Disable** XHCI Hand-off This is a workaround for OSes without XHCI hand-off support. The XHCI ownership change should be claimed by XHCI driver.
USB Mass Storage Driver Support	**Enable** (default) or **Disable** USB Mass Storage Driver Support.

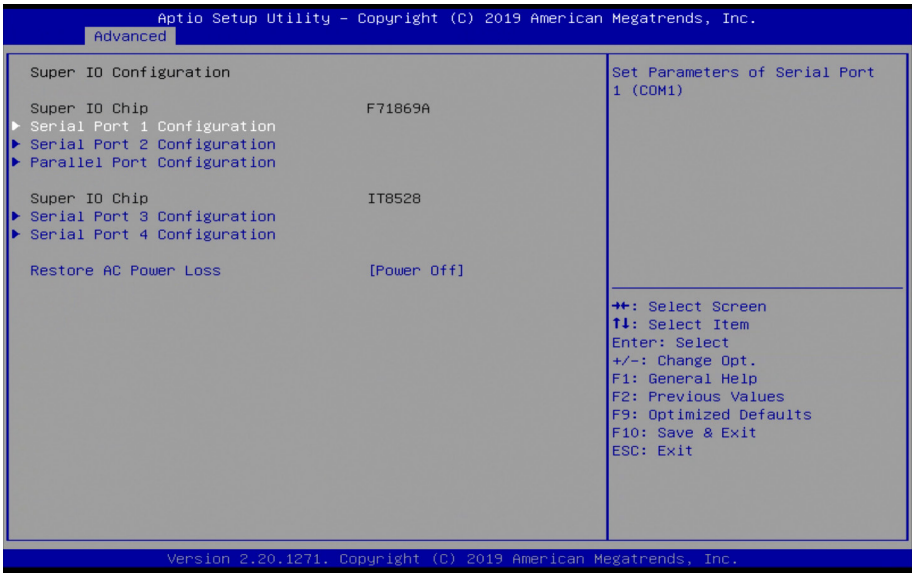
USB hardware delay and time-out	
USB Transfer time-out	Use this item to set the time-out value for control, bulk, and interrupt transfers. ► Options available are: **1 sec, 5 sec, 10 sec, 20 sec** (default)
Device reset time-out	Use this item to set USB mass storage device start unit command time-out. ► Options available a re: **10 sec, 20 sec** (default)**, 30 sec, 40 sec**
Device power-up delay	Use this item to set maximum time the device will take before it properly reports itself to the host controller. ► Options available are: **Auto** (Default): 'Auto' uses default value: for a root port it is 100 ms, for a hub port the delay is taken from hub descriptor. **Manual**: Select **Manual** you can set value for the following sub-item: '**Device Power-up delay in seconds**', the delay range in from 1 to 40 seconds, in one second increments.

4.2.9 Network Stack Configuration



Setting	Description
Network Stack	Enables/disables UEFI network stack. ► **Disabled** is the default.

4.2.10 Super IO Configuration



Setting	Description
Serial Port 1/2/3/4 & Parallel Port Configuration	See next page.
Restore AC Power Loss	Specify what state to go to when power is re-applied after a power failure. ► Options: **Last State**, **Power On** and **Power Off** (default)

Serial Port 1/2/3/4 Configuration

Setting	Description
Serial Port	**Enable** (default) or **Disable** Serial Port (COM).
Change Settings	Select an optimal setting for Super IO device. ► Options for Serial Port 1: **Auto**; **IO=3F8h; IRQ=4** (default) ; **IO=2F8h; IRQ=3, 4, 7, 10, 11, 12**; ► Options for Serial Port 2: **Auto** **IO=2F8h; IRQ=3** (default) **IO=3F8h; IRQ=3, 4, 7, 10, 11, 12** ► Options for Serial Port 3: **Auto** **IO=3E8h; IRQ=11** (default) **IO=2E8h; IRQ=3, 4, 7, 10, 12** ► Options for Serial Port 4: **Auto** **IO=2E8h; IRQ=10** (default) **IO=3E8h; IRQ=3, 4, 7, 10, 12**

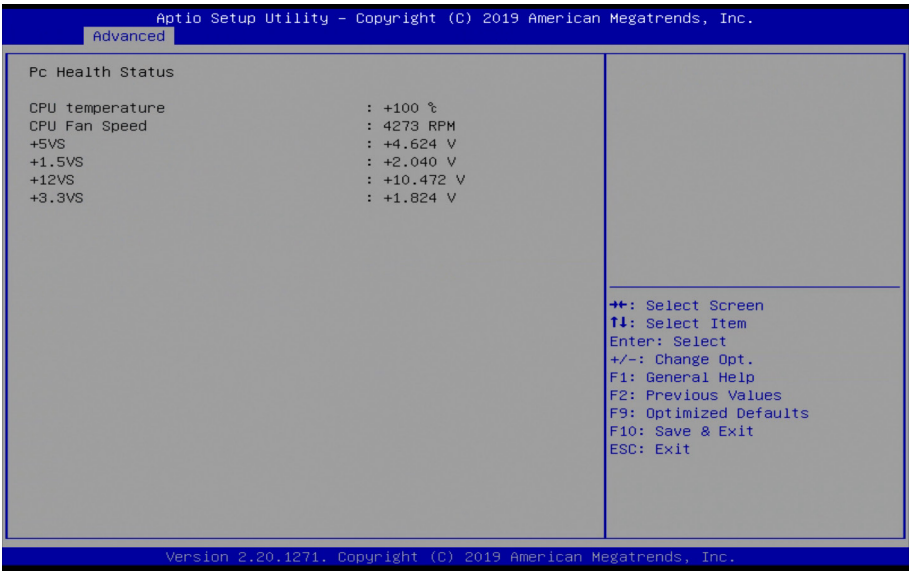
Parallel Port Configuration

Setting	Description
Parallel Port	**Enable** (default) or **Disable** Parallel Port (LPT/LPTE).
Change Settings	Select an optimal setting for Super IO device. ► Options: **Auto** **IO=378h; IRQ=7** (default) **IO=378h; IRQ=7, 10, 11, 12;** **IO=278h; IRQ=7, 10, 11, 12;** **IO=3BCh; IRQ=7, 10, 11, 12;**

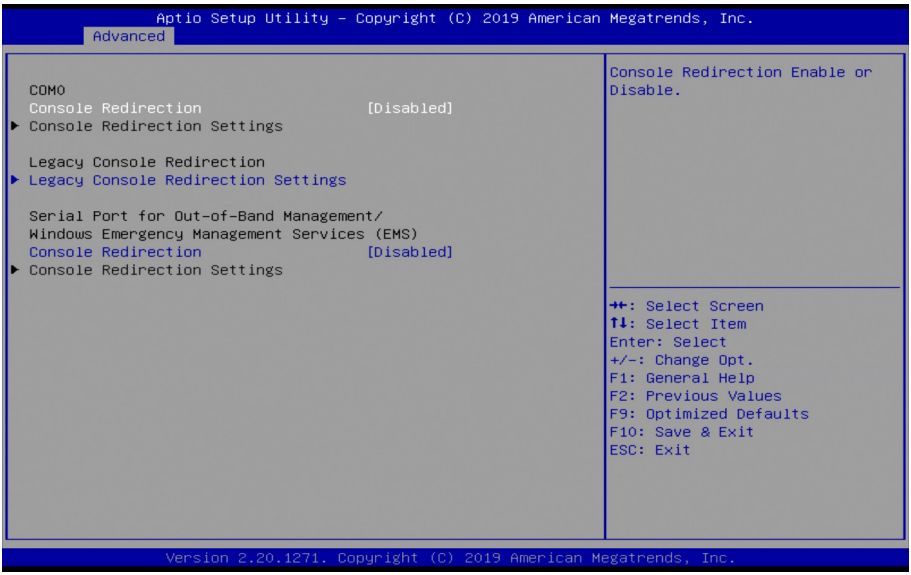
Device Mode (only for Parallel Port Configuration)	Change the Printer Port mode. ► Options: **STD Printer Mode** (default) **SPP Mode** **EPP-1.9 and SPP Mode** **EPP-1.7 and SPP Mode** **ECP Mode** **ECP and EPP 1.9 Mode** **ECP and EPP 1.7 Mode**.

4.2.11 H/W Monitor

Access this page to view the hardware information.



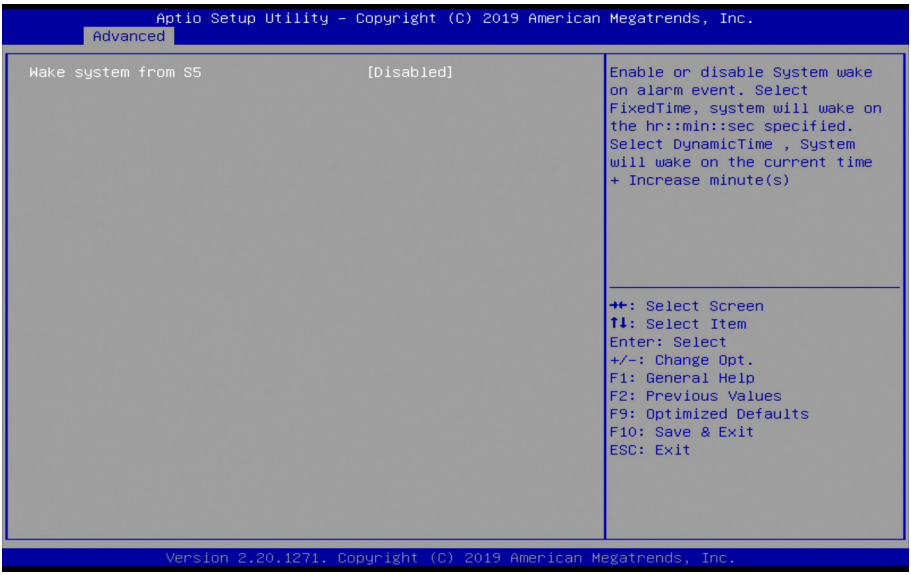
4.2.12 Serial Port Redirection



Setting	Description
Console Redirection	**Enable** or **Disable** (default) console redirection. Following submenu is available only when **Console Redirection** is set to **Enabled**.
Legacy Console Redirection Settings	
Redirection COM Port	Select a COM port to display redirectino of Legacey OS and Legacy OPROM message. ► **COM0** is the default.
Resolution	On legacy OS, the Number of Rows and Columns supported redirection. ► **80x24** is the default.

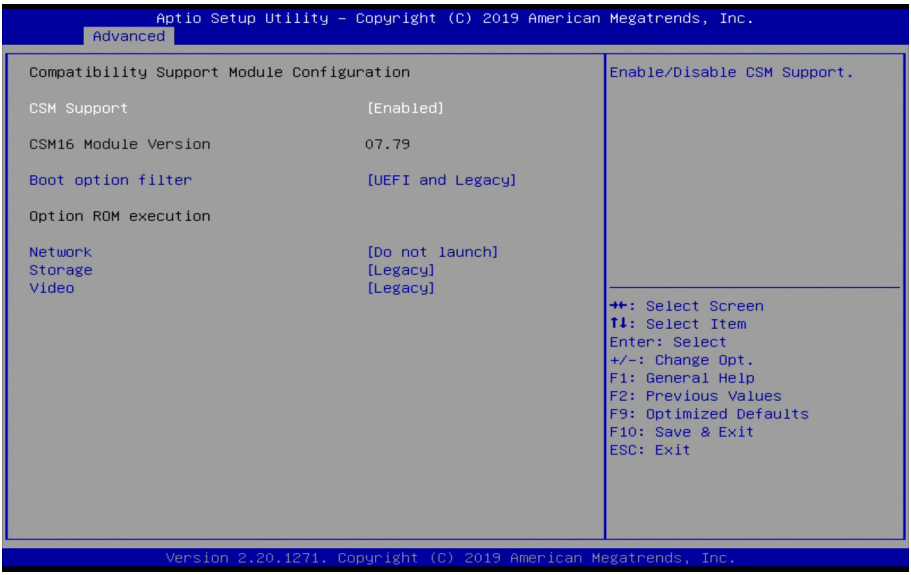
Redirect After POST	When Bootloader is selected, then Legacy Console Redirection is disabled before booting to legacy OS. When Always Enable is selected, then Legacy Console Redirection is enabled for legacy OS. Default settinf for this option is set to Always Enable ▸ Options available are: **Always Enable**(default): set the Redirection to be always active **Boot Loader**: set the Redirection to be active during POST and Boot Loader
Console Redirection	Enables/Disables console redirection. ▸ **Disabled** is the default. ▸ Following submenu is available only when **Console Redirection** is set to **Enabled**.

4.2.13 S5 RTC Wake Settings



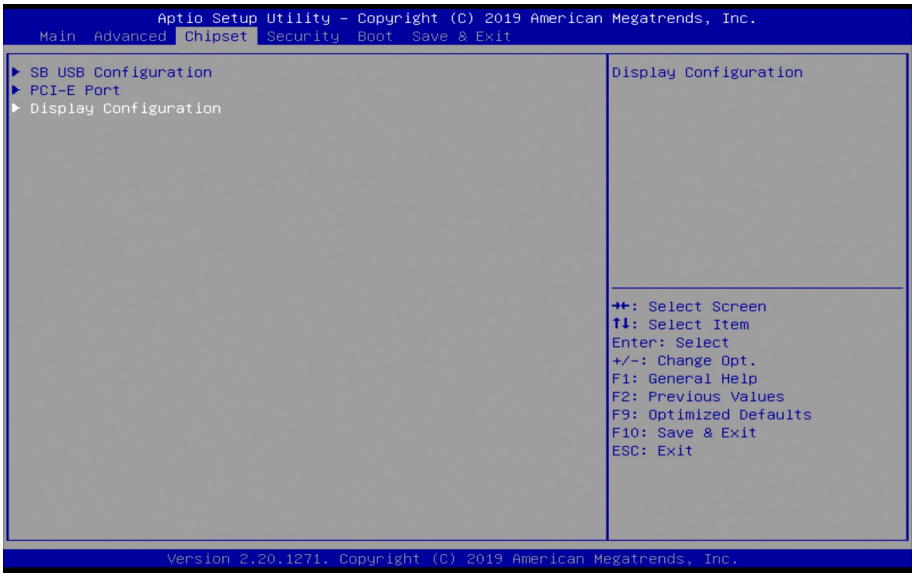
Setting	Description
Wake System from S5	**Enable** or **Disable** (default) system wake on alarm event. ► Options available are: **Disabled** (default): **Fixed Time:** System will wake on the hr::min::sec specifiedc. **DynamicTime:** If selected, you need to set **Wake up minute increase** from 1 - 5. System will wake on the current time + increase minute(s).

4.2.14 CSM Configuration



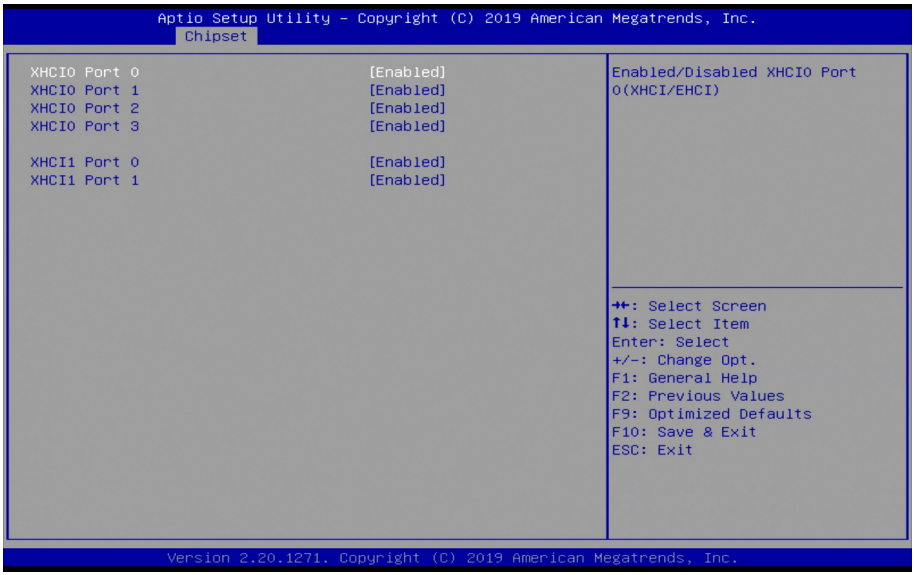
Setting	Description
CSM Support	**Enable** (default) or **Disable** CSM Support.
Boot option filter	Control the Legacy/UEFI ROMs priority. ► Options: **UEFI and Legacy** (default), **Legacy only** and **UEFI only**
Network	Control the execution of UEFI and Legacy PXE OpROM ► Options: **Do not lauch** (default), **UEFI** and **Legacy**
Storage	Control the execution of UEFI and Legacy Storage OpROM ► Options: **Do not lauch**, **UEFI** and **Legacy** (default)
Video	Control the execution of UEFI and Legacy Video OpROM ► Options: **Do not lauch**, **UEFI** and **Legacy** (default)

4.3 Chipset



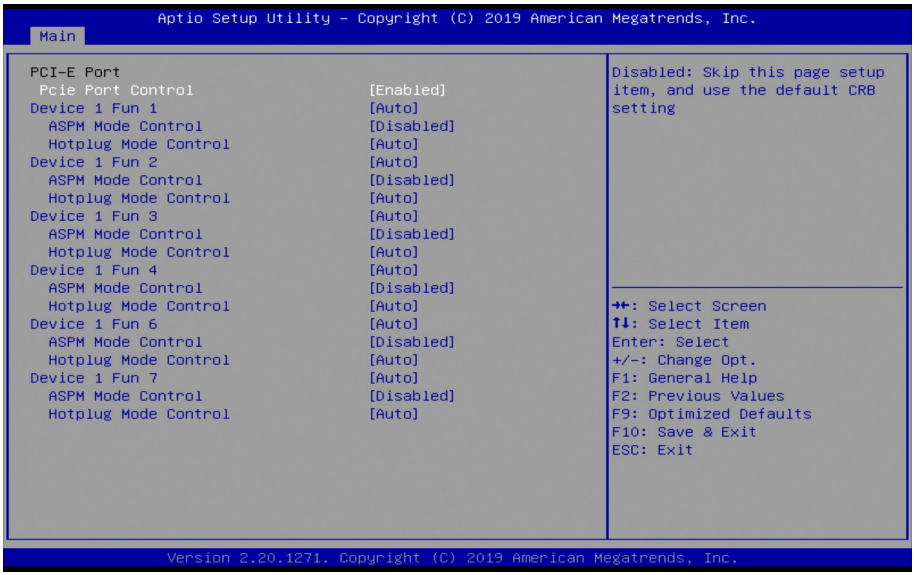
Setting	Description
SB USB Configuratoin	See 4.3.1 SB USB Config on page 42
PCI-E Port	See 4.3.2 PCI-E Port on page 43
Display Configuration	See 4.3.2 Display Configuration on page 44

4.3.1 SB USB Config



Setting	Description
XHCI0 Port 0~3	**Enable** (default) /**disable** (default) xHCI0 port 0~3.
XHCI1 Port 0~1	**Enable** (default) /**disable** (default) xHCI1 port 0~1.

4.3.2 PCI-E Port



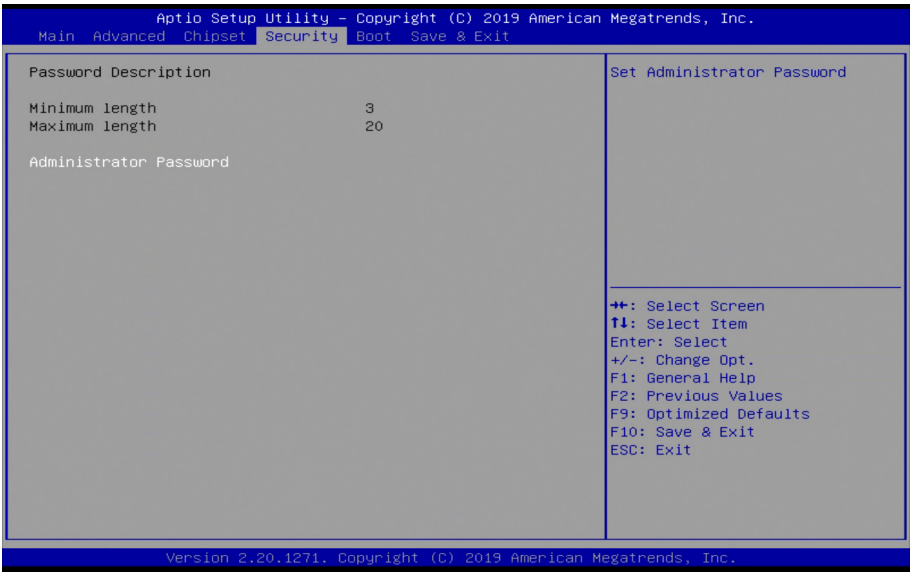
Setting	Description
PCIe Port Control	**Enable** (default) or **disable** the PCIe port.
Device 1 Fun1~7	Select Device 1 function. ► Options: **Auto** (default), **Disabled**, and **Enabled**
ASPM Support	Disable or set the ASPM level. Force L0s will force all inks to L0s state. “Auto” will allow BIOS to auto configure.”Disable” will disable ASPM. ► Options: **Disabled** (default), **L0s Entry**, **L1 Entry**, **L0s and L1 Entry** and **Auto**.
Hot Plug Mode Control	NB Root port hogplug mode control. ► Options: **Disabled**, **Hotplug Basic**, **Hotplug Server**, **Hotplug Enhanced**, **Hotplug Inboard** and **Auto** (default)

4.3.3 Display Configuration

Item	Description
Active LVDS	**Enable** or **Disable** (\default) active LVDS control.

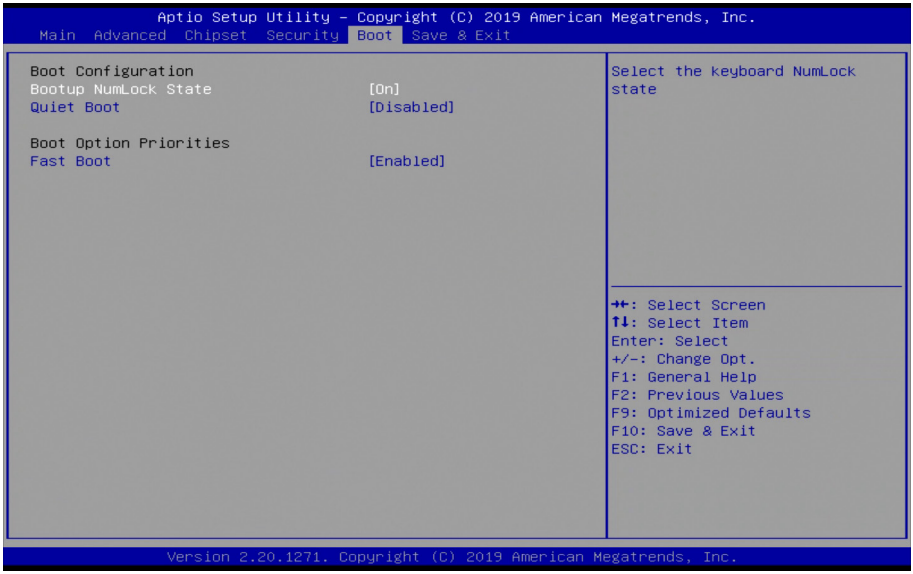
4.5 Security

The **Security** menu sets up the administrator password.



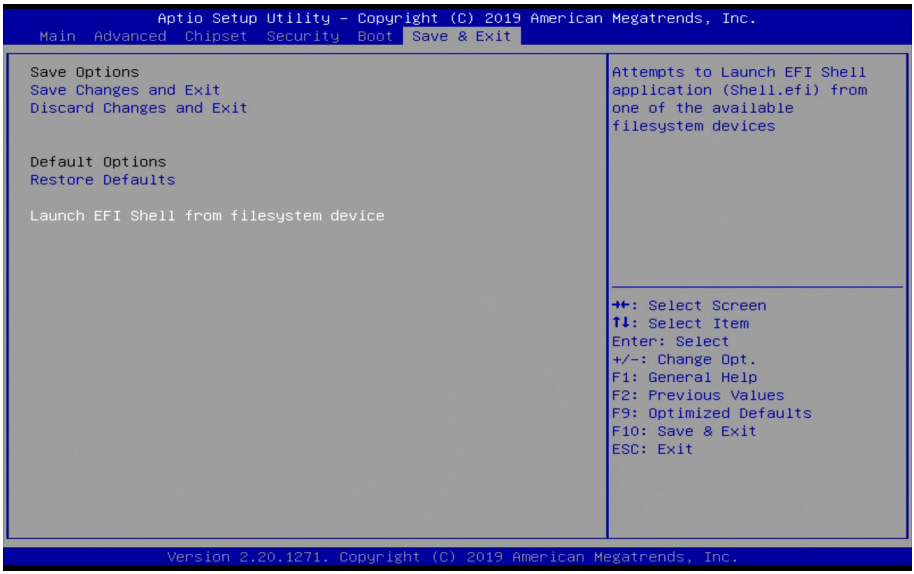
Setting	Description
Administrator Password	To set up an administrator password: 1. Select **Administrator Password**. The screen then pops up an **Create New Password** dialog. 2. Enter your desired password that is no less than 3 characters and no more than 20 characters. 3. Hit [Enter] key to submit.

4.6 Boot



Setting	Description
Boot NumLock State	Select the keyboard NumLock state. ► Options: **On** and **Off** (default).
Quiet Boot	**Enable** or **Disable** (default) Quiet Boot option.
Fast Boot	**Enable** or **Disable** (default) boot with initialization of a minimal set of devices required to launch active boot option. Has no effect for BBS boot options.

4.6 Save & Exit



Setting	Description
Save Changes and Exit	Exit system setup after saving the changes. ► Enter the item and then a dialog box pops up: **Save configuration and exit? (Yes/ No)**
Discard Changes and Exit	Exit system setup without saving the changes. ► Enter the item and then a dialog box pops up: **Quit without saving? (Yes/ No)**
Restore Defaults	Restore/Load Default values for all the setup options. ► Enter the item and then a dialog box pops up: **Load Optimized Defaults? (Yes/ No)**
Launch EFI Shell from fi.lesystem device	Attempts to launch EFI shell application (Shell.efi) from one of the available filesystem devices.

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Appendix

Appendix A: I/O Port Address Map

Each peripheral device in the system is assigned a set of I/O port addresses which also becomes the identity of the device. The following table lists the I/O port addresses used.

Address	Device Description
03F8-03FF	Communications Port (COM1)
02F8-02FF	Communications Port (COM2)
002E-002F	Motherboard resources
004E-004F	Motherboard resources
0061-0061	Motherboard resources
0070-0071	Motherboard resources
0080-0080	Motherboard resources
0092-0092	Motherboard resources
00B2-00B3	Motherboard resources
1800-18FE	Motherboard resources
0A00-0A1F	Motherboard resources
0A20-0A2F	Motherboard resources
0A30-0A3F	Motherboard resources
0800-089F	Motherboard resources
0C00-0C01	Motherboard resources
0C50-0C51	Motherboard resources
0CD0-0CD1	Motherboard resources
0CD4-0CD5	Motherboard resources
0CD6-0CD7	Motherboard resources
0CD8-0CDF	Motherboard resources
0CF8-0CFF	PCI Express Configuration Access Port
0378-037F	Printer Port (LPT1)
0020-0021	Programmable interrupt controller
00A0-00A1	Programmable interrupt controller
04D0-04D1	Programmable interrupt controller

0040-0043	System timer
0B00-0B1F	SM Bus 0 Controller
0B20-0B3F	SM Bus 1 Controller
FE00-FEFF	Standard SATA AHCI Controller
FF00-FF1F	Standard SATA AHCI Controller

Appendix B: BIOS Memory Mapping

Address	Device Description
0xDF000000-0xDF01FFFF	Ethernet Controller
0xDF040000-0xDF043FFF	High Definition Audio Controller
0xDF020000-0xDF02FFFF	High Definition Audio Controller
0xFED00000-0xFED003FF	High Precision Event Timer
0xFF000000-0xFFFFFFFF	Intel 82802 Firmware Hub Device
0xDF030000-0xDF03FFFF	Intel USB 3.0 eXtensible Host Controller - 0100 (Microsoft)
0xA0000-0xBFFFF	Microsoft Basic Display Adapter
0xDE000000-0xDEFFFFFF	Microsoft Basic Display Adapter
0xC0000000-0xCFFFFFFF	Microsoft Basic Display Adapter
0xFED10000-0xFED17FFF	Motherboard resources
0xFED18000-0xFED18FFF	Motherboard resources
0xFED19000-0xFED19FFF	Motherboard resources
0xE0000000-0xEFFFFFFF	Motherboard resources
0xFED90000-0xFED93FFF	Motherboard resources
0xFED45000-0xFED8FFFF	Motherboard resources
0xFEE00000-0xFEEFFFFF	Motherboard resources
0xDFFE0000-0xDFFFFFFF	Motherboard resources
0xFE029000-0xFE029FFF	Motherboard resources
0xFE028000-0xFE028FFF	Motherboard resources
0xFDAF0000-0xFDAFFFFF	Motherboard resources
0xFDAE0000-0xFDAEFFFF	Motherboard resources
0xFDAC0000-0xFDACFFFF	Motherboard resources
0xFD000000-0xFDABFFFF	Motherboard resources
0xFDAD0000-0xFDADFFFF	Motherboard resources
0xFDB00000-0xFDFFFFFF	Motherboard resources
0xFE000000-0xFE01FFFF	Motherboard resources
0xFE036000-0xFE03BFFF	Motherboard resources
0xFE03D000-0xFE3FFFFF	Motherboard resources

0xFE410000-0xFE7FFFFF	Motherboard resources
0x00030000-0x0006FFFF	Motherboard resources
0x80000000-0x8FFFFFFF	Motherboard resources
0xFEB00000-0xFEB0FFFF	Motherboard resources
0xFEB80000-0xFEBFFFFF	Motherboard resources
0xFEC01000-0xFEC01FFF	Motherboard resources
0xFEC30000-0xFEC3FFF	Motherboard resources
0xFED00000-0xFED02FFF	Motherboard resources
0xFED40000-0xFED44FFF	Motherboard resources
0xFEDC9000-0xFEDC9FFF	Motherboard resources
0xFEDCA000-0xFEDCAFFF	Motherboard resources
0xFF000000-0xFFFFFFFF	Motherboard resources
0xDF051000-0xDF051FFF	PCI Data Acquisition and Signal Processing Controller
0xFD000000-0xFDABFFFF	PCI Express Root Complex
0x90000000-0xDFFFFFFF	PCI Express Root Complex
0xDF044000-0xDF047FFF	PCI Memory Controller
0xDF04B000-0xDF04BFFF	SDA Standard Compliant SD Host Controller
0xF0F0F000 - 0xF0F1FFFF	Standard SATA AHCI Controller
0xF8000000 - 0xFBFFFFFF	PCI Express Root Complex
0xFE400000 - 0xFE40FFFF	XHCI Controller
0xFEC00000 - 0xFEC00FFF	APIC
0xFEC10000 - 0xFEC1FFF	SPI

Appendix C: Interrupt Request Lines (IRQ)

Peripheral devices use interrupt request lines to notify CPU for the service required. The following table shows the IRQ used by the devices on board.

Level	Function
IRQ0	System timer
IRQ1	PS/2 Keyboard
IRQ3	Communications Port (COM2)
IRQ4	Communications Port (COM1)
IRQ5	SM Bus Controller
IRQ8	System CMOS/real time clock
IRQ10	Communications Port (COM4)
IRQ11	Communications Port (COM3)
IRQ12	PS/2 Mouse
IRQ16~IRQ31	PCIe Devices

Appendix D: Watchdog Timer (WDT) Setting

WDT is widely used for industry application to monitor the activity of CPU. Application software depends on its requirement to trigger WDT with adequate timer setting. Before WDT time out, the functional normal system will reload the WDT. The WDT never time out for a normal system. The WDT will not be reloaded by an abnormal system, then WDT will time out and reset the system automatically to avoid abnormal operation.

This board supports 255 levels watchdog timer by software programming I/O ports. Below are the source codes written in C, please take them as WDT application example.

```
/*--------------------------------------------------------------------------*/
#include <math.h>
#include <stdio.h>
#include <dos.h>

int iWDTCount;

int sioIndex  = 0x2E;     // or 0x4E
int sioData   = 0x2F;     // or 0x4F

int main(void)
{
    unsigned char          iCount;

    printf("WDT Times ( 1 ~ 255 ) : ");
    scanf("%d",&iCount);
    printf("\n");

    WDT_Start(iCount);

    return 0;
}

void WDT_Start(int iCount)
{
    int iData;

    outportb(sioIndex, 0x87);      /* Enable Super I/O */
    outportb(sioIndex, 0x87);

     outportb(sioIndex, 0x07);     /* Select logic device - WDT */
     outportb(sioData,  0x07);

     outportb(sioIndex, 0x29);     /* Enable WDTRST# Pin */
     iData = inportb(sioData);
     iData = iData & 0xEF;
     outportb(sioData,  iData);    /* The pin function is WDTRST# */

     outportb(sioIndex, 0x30);     /* Enable WDT */
     outportb(sioData,  0x01);
```

```
    outportb(sioIndex, 0xF0);      /* Enable WDTRST# Output */
    outportb(sioData,  0x80);

   iWDTCount = iCount;
    outportb(sioIndex, 0xF6);      /* Set WDT Timeout value */
    outportb(sioData,  iCount);

    outportb(sioIndex, 0xF5);      /* Set Configure and Enable WDT timer, Start
countdown */
    outportb(sioData,  0x32);

   outportb(sioIndex, 0xAA);       /* Disable Super I/O */
}

void WDT_Stop(void)
{
   outportb(sioIndex, 0x87);       /* Enable Super I/O */
   outportb(sioIndex, 0x87);

    outportb(sioIndex, 0x07);      /* Select logic device - WDT */
    outportb(sioData,  0x07);

   outportb(sioIndex, 0xF5);       /* Disable WDT timer, stop countdown */
   outportb(sioData,  0x12);

   outportb(sioIndex, 0xAA);       /* Disable Super I/O */
}

void SioWDTClear(void)
{
   outportb(sioIndex, 0x87);       /* Enable Super I/O */
   outportb(sioIndex, 0x87);

    outportb(sioIndex, 0x07);      /* Select logic device - WDT */
    outportb(sioData,  0x07);

   outportb(sioIndex, 0xF6);       /* Reset WDT Timeout Value */
   outportb(sioData,  iWDTCount);

   outportb(sioIndex, 0xAA);       /* Disable Super I/O */
}

int SioWDTCount(void)
{
    int iData;

   outportb(sioIndex, 0x87);       /* SIO - Enable */
   outportb(sioIndex, 0x87);

    outportb(sioIndex, 0x07);      /* LDN - WDT */
    outportb(sioData,  0x07);

    outportb(sioIndex, 0xF6);      /* WDT - Timeout Value */
    iData = inportb(sioData);
```

```
    outportb(sioIndex, 0xAA);      /* SIO - Disable */

    return iData;
}
```

Appendix D: DIO Sample Code

```
/*---------------------------------------------------------------------------*/
#include "math.h"
#include "stdio.h"
#include "dos.h"

/* SM Bus */
int SMB_PORT_AD    = 0xB00;
int SMB_DEVICE_ADD = 0x40;              /* TCA6408A's Add = 6eh or 9ch */

int main(void)
{
   int iInput;

   GPIOMode(0xF0);
   delay(10000);

   GPIOData(0x0A);
   delay(30000);
   iInput = GPIOStatus();
   printf(" Data : %2x \n",iInput);

   GPIOData(0x05);
   delay(30000);
   iInput = GPIOStatus();
   printf(" Data : %2x \n",iInput);

   return 0;
}

void GPIOMode(int iMode)
{
   SMB_Byte_WRITE(SMB_PORT_AD,SMB_DEVICE_ADD,0x03,iMode);    /* DIO 0 ~ 7 Mode */
}

void GPIOData(int iData)
{
   SMB_Byte_WRITE(SMB_PORT_AD,SMB_DEVICE_ADD,0x01,iData);    /* DIO 0 ~ 7 Data */
}

int GPIOStatus()
{
   int iStatus;

   iStatus = SMB_Byte_READ(SMB_PORT_AD,SMB_DEVICE_ADD,0x00);/* DIO 0 ~ 7 Status
*/

   return iStatus;
}
```