EmETXe-i87M0

COM Express® Compact Type 6 CPU Module

User's Manual

Version 1.1

2016.04

Revision History

Version	Date	Description
1.0	2013/12	initial release
1.1	2016/04	P.4 Add HS-87M2-C2

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Copyright Notice

The information in this document is subject to change without prior notice in order to improve the reliability, design and function. It does not represent a commitment on the part of the manufacturer.

Under no circumstances will the manufacturer be liable for any direct, indirect, special, incidental, or consequential damages arising from the use or inability to use the product or documentation, even if advised of the possibility of such damages.

Declaration of Conformity

CE

The CE symbol on your product indicates that it is in compliance with the directives of the Union European (EU). A Certificate of Compliance is available by contacting Technical Support.

This product has passed the CE test for environmental specifications when shielded cables are used for external wiring. We recommend the use of shielded cables. This kind of cable is available from ARBOR. Please contact your local supplier for ordering information.

This product has passed the CE test for environmental specifications. Test conditions for passing included the equipment being operated within an industrial enclosure. In order to protect the product from being damaged by ESD (Electrostatic Discharge) and EMI leakage, we strongly recommend the use of CE-compliant industrial enclosure products.

> Warning
>
> This is a class A product. In a domestic environment this product may cause radio interference in which case the user may be required to take adequate measures.

FCC Class A

This device complies with Part 15 of the FCC Rules. Operation is subject to the following two conditions:

(1)This device may not cause harmful interference, and

(2)This device must accept any interference received, including interference that may cause undesired operation.

NOTE:

This equipment has been tested and found to comply with the limits for a Class A digital device, pursuant to Part 15 of the FCC Rules. These limits are designed to provide reasonable protection against harmful interference when the equipment is operated in a commercial environment. This equipment generates, uses, and can radiate radio frequency energy and, if not installed and used in accordance with the instruction manual, may cause harmful interference to radio communications. Operation of this equipment in a residential area is likely to cause harmful interference in which case the user will be required to correct the interference at his own expense.

RoHS

ARBOR Technology Corp. certifies that all components in its products are in compliance and conform to the European Union's Restriction of Use of Hazardous Substances in Electrical and Electronic Equipment (RoHS) Directive 2002/95/EC.

The above mentioned directive was published on 2/13/2003. The main purpose of the directive is to prohibit the use of lead, mercury, cadmium, hexavalent chromium, polybrominated biphenyls (PBB), and polybrominated diphenyl ethers (PBDE) in electrical and electronic products. Member states of the EU are to enforce by 7/1/2006.

ARBOR Technology Corp. hereby states that the listed products do not contain unintentional additions of lead, mercury, hex chrome, PBB or PBDB that exceed a maximum concentration value of 0.1% by weight or for cadmium exceed 0.01% by weight, per homogenous material. Homogenous material is defined as a substance or mixture of substances with uniform composition (such as solders, resins, plating, etc.). Lead-free solder is used for all terminations (Sn(96-96.5%), Ag(3.0-3.5%) and Cu(0.5%)).

SVHC / REACH

To minimize the environmental impact and take more responsibility to the earth we live, Arbor hereby confirms all products comply with the restriction of SVHC (Substances of Very High Concern) in (EC) 1907/2006 (REACH --Registration, Evaluation, Authorization, and Restriction of Chemicals) regulated by the European Union.

All substances listed in SVHC < 0.1 % by weight (1000 ppm)

Warning

Single Board Computers and their components contain very delicate Integrated Circuits (IC). To protect the Single Board Computer and its components against damage from static electricity, you should always follow the following precautions when handling it :

1. Disconnect your Single Board Computer from the power source when you want to work on the inside.

2. Hold the board by the edges and try not to touch the IC chips, leads or circuitry.

3. Use a grounded wrist strap when handling computer components.

4. Place components on a grounded antistatic pad or on the bag that comes with the Single Board Computer, whenever components are separated from the system.

Replacing the Lithium Battery

Incorrect replacement of the lithium battery may lead to a risk of explosion.

The lithium battery must be replaced with an identical battery or a battery type recommended by the manufacturer.

Do not throw lithium batteries into the trash-can. It must be disposed of in accordance with local regulations concerning special waste.

Technical Support

If you have any technical difficulties, please consult the user's manual first at: ftp://ftp.arbor.com.tw/pub/manual
Please do not hesitate to call or e-mail our customer service when you still cannot find out the answer.

http://www.arbor.com.tw
E-mail:info@arbor.com.tw

Warranty

This product is warranted to be in good working order for a period of two years from the date of purchase. Should this product fail to be in good working order at any time during this period, we will, at our option, replace or repair it at no additional charge except as set forth in the following terms. This warranty does not apply to products damaged by misuse, modifications, accident or disaster.

Vendor assumes no liability for any damages, lost profits, lost savings or any other incidental or consequential damage resulting from the use, misuse of, or inability to use this product. Vendor will not be liable for any claim made by any other related party.

Vendors disclaim all other warranties, either expressed or implied, including but not limited to implied warranties of merchantability and fitness for a particular purpose, with respect to the hardware, the accompanying product's manual(s) and written materials, and any accompanying hardware. This limited warranty gives you specific legal rights.

Return authorization must be obtained from the vendor before returned merchandise will be accepted. Authorization can be obtained by calling or faxing the vendor and requesting a Return Merchandise Authorization (RMA) number. Returned goods should always be accompanied by a clear problem description.

Chapter 1

Introduction

1.1 The Product

The EmETXe-i87M0 is a space-conscious CPU board of 125 mm x 95 mm to take up only small footprint in your system. By the architecture of Type 6, the board has two high-performance connectors to promise stable data passing rate. The soldered onboard Intel® 4th Generation Core™ processor, along with integrated Intel® HD Graphics Gen 7.5 graphics chipset, bring Analog RGB, LVDS and DDI solution for most CRT monitors or LCD video panels.

For system configuration, the board is supported by AMI UEFI BIOS. EmETXe-i87M0 is an ideal choice for some demanding industrial control and data communications by its significant processing performance, low power consumption and these features:

- Soldered onboard Intel® 4th Generation Core™ processor
- Integrated Gigabit Ethernet
- Dual-channel 24-bit LVDS, analog RGB, and 3 x DDI ports
- Supports 3 independent displays
- RAID 0, 1, 5, 10 supported
- Support Intel® Active Management Technology (Intel AMT)
- Extended Operating Temp.: -20 ~ 70°C

1.2 About This Manual

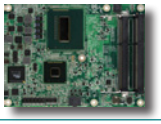
This user's manual provides general information and installation instructions about the product. This user's manual is intended for experienced users and integrators with hardware knowledge of personal computers. If you are not sure about any description in this booklet. Please consult your vendor before further handling.

1.3 Specifications

System	
CPU	Intel® 4th Generation Core™ i5 4402E 1.6GHz processor
Memory	2 x DDR3L SO-DIMM sockets, supporting up to 16GB SDRAM
Chipset	Intel® PCH QM87
BIOS	AMI® UEFI BIOS
Watchdog Timer	1~255 levels reset
I/O	
USB Port	12 x USB ports: - 8 x USB 2.0 ports - 4 x USB 3.0 ports
Digital I/O	8-bit programmable Digital Input/Output
Storage	4 x serial ATA ports: - 2 ports with 600MB/s HDD transfer rate - 2 ports with 300MB/s HDD transfer rate
	SATA RAID 0, 1, 5, 10 supported
Expansion Bus	1 x PCIe x16 Gen3 lanes
	8 x PCIe x1 Gen2 lanes
Ethernet Chipset	1 x Intel® I217 PCIe GbE PHY
Audio	HD Audio link
Display	
Graphics Chipset	Integrated Intel® HD Graphics Gen 7.5
Graphics Interface	Analog RGB supports up to 1920x1200@60Hz
	LCD: Dual Channels 24-bit LVDS up to 1920 x 1200 @60Hz
	3 x DDI port
Mechanical & Environmental	
Power Requirement	+12V
Power Consumption	2.07A @+12V (with 37W, B0 ES sample)
Operating Temp.	-20 ~ 70°C (-4 ~ 158°F)
Operating Humidity	10 ~ 95% @ 60ºC (non-condensing)
Dimension (L x W)	125 x 95 mm (4.9” x 3.7”)

1.4 Inside the Package

Before you begin installing your single board, please make sure that the following materials have been shipped:



1 x EmETXe-i87M0 COM Express CPU Module

1 x Driver CD
1 x Quick Installation Guide

If any of the above items is damaged or missing, contact your vendor immediately.

1.5 Ordering Information

EmETXe-i87M0-4402E	Intel® 4th Generation Core™ i5-4402E/ QM87 COM Express CPU module

1.5.1 Optional Accessories

HS-87M0-F1	Heat spreader (125x95x18mm)
HS-87M0-F2	Heat spreader (95x95x11mm)
HS-0000-W4	Universal evaluation heat sink kit w/ thermal pad (Dimensions: 125x95x22mm, only used on a flat-type heat spreader)
HS-87M2-C2	Cooler 125x95x34mm
PBE-1702	COM Express type 6 evaluation carrier board (ATX form factor)
CBK-04-1702-00	Cable Kit • 1 x SATA cable • 2 x COM port cables • 1 x USB cable

1.6 The Installation Paths of CD Driver

The CPU module supports Windows 7 and 8. Find the necessary drivers on the CD that comes with your purchase. For different OS, the driver installation may vary slightly, but generally they are similar. **DO** install **Chipset→Graphic→Audio** before the rest to prevent errors.

Find the drivers on CD by the following paths:

Windows 8

Driver	Path
Chipset	EmETXe-i87M0\Chipset
Graphic	EmETXe-i87M0\Graphic\32 Bit\Win32_V9.18.10.3107
	EmETXe-i87M0\Graphic\64 Bit\win64_V9.18.10.3107
Audio	EmETXe-i87M0\Audio\win7_win8\32Bit
	EmETXe-i87M0\Audio\win7_win8\64Bit
LAN	EmETXe-i87M0\Ethernet\Win8\32Bit
	EmETXe-i87M0\Ethernet\Win8\64Bit
ME	EmETXe-i87M0\ME\ME9.0_5M_V9.0.2.1345

Windows 7

Driver	Path
Chipset	EmETXe-i87M0\Chipset
Graphic	EmETXe-i87M0\Graphic\32 Bit\Win32_V9.18.10.3107
	EmETXe-i87M0\Graphic\64 Bit\win64_V9.18.10.3107
Audio	EmETXe-i87M0\Audio\win7_win8\32Bit
	EmETXe-i87M0\Audio\win7_win8\64Bit
LAN	EmETXe-i87M0\Ethernet\Win7\32Bit
	EmETXe-i87M0\Ethernet\Win7\64Bit
ME	EmETXe-i87M0\ME\ME9.0_5M_V9.0.2.1345
USB3.0	EmETXe-i87M0\USB 3.0\USB3_V2.5.0.19

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Chapter 2

Board Overview

2.1 What Is "COM Express®"?

With more and more demands on small and embedded industrial boards, a multi-functional COM (Computer-on-Module) surfaces as a great solution.

COM Express® supports seven pin-out types applying to Basic and Extended form factors:

Module Type 1 and 10 support single connector with two rows (220 pins).

Module Type 2, 3, 4, 5 and 6 support two connectors with four rows (440 pins).

EmETXe-i87M0 is a Type-6 module.

Difference between Standard Type 6 and EmETXe-i87M0 is listed as below:

Module Type	Standard Type 6	EmETXe-i87M0
Connectors	2	2
Connector Rows	A, B, C, D	A, B, C, D
PCIe Lanes (Max)	24	24
LAN (Max)	1	1
Serial Ports (Max)	2	0
Digital Display I/F (Max)	3	3
USB 3.0 Ports (Max)	4	4

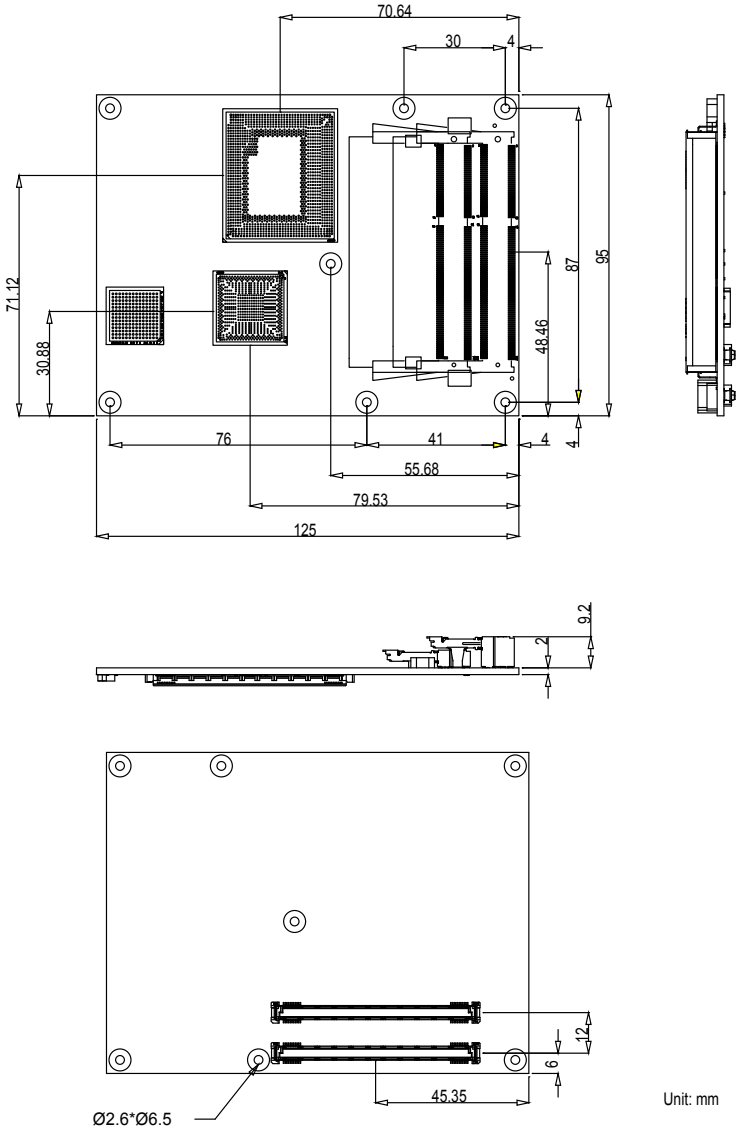
Row AB provides pins for PCI Express, SATA, LVDS, LCD channel, LPC bus, system and power management, VGA, LAN, and power and ground interfaces.

Row CD provides SDVO and legacy PCI and IDE signals next to additional PCI Express, LAN and power and ground signals. The COM are targeted at following applications:

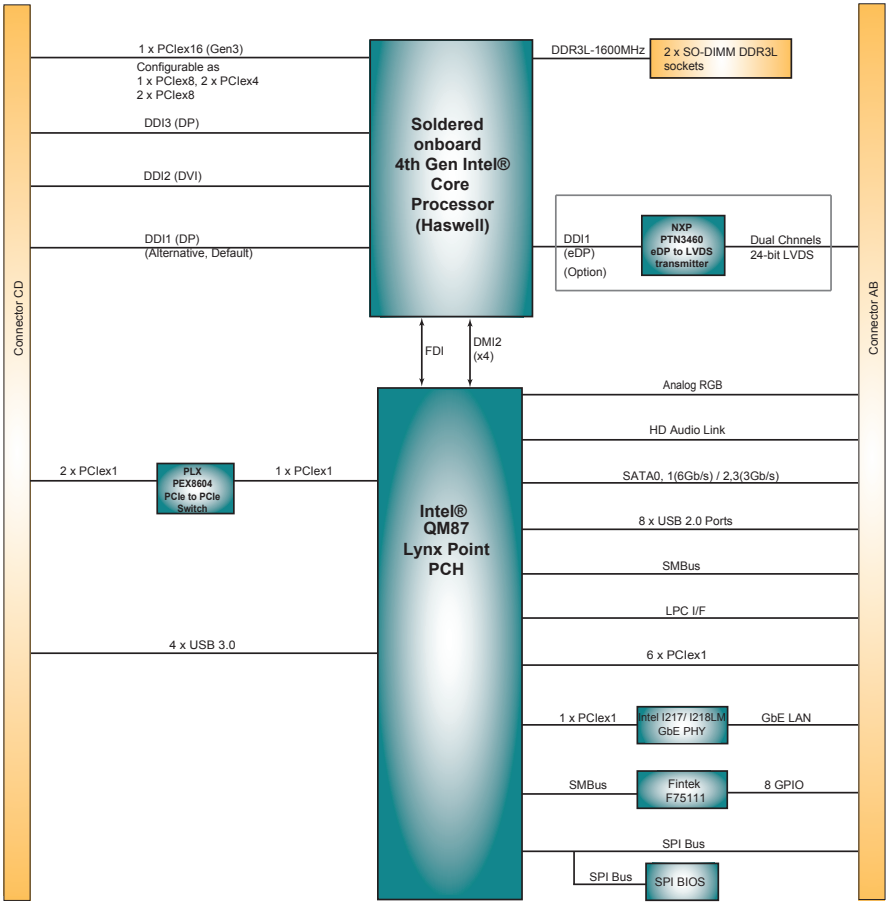
- Retail & Advertising
- Medical
- Test & Measurement
- Gaming & Entertainment
- Industrial & Automation
- Military & Government
- Security

2.2 Board Dimensions

The following illustration shows the dimension of EmETXe-i87M0, with the measurements in width, depth, and height called out.



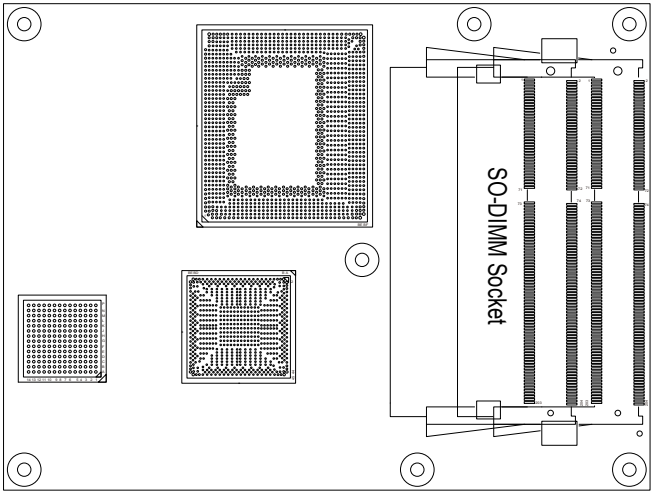
2.3 Block Diagram



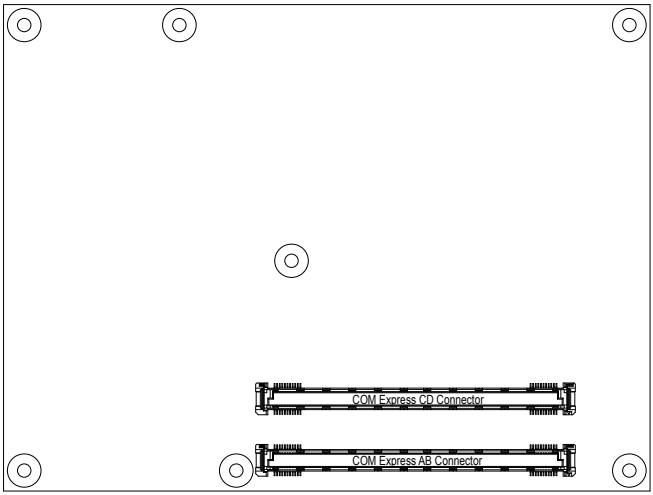
2.4 Connector Pin Definition

Being a most commonly-used Type 6, the EmETXe-i87M0 features two board-to-board connectors on bottom side.

Top Side



Bottom Side



COM Express AB Connector (bottom side)

B1	GND (FIXED)	GND (FIXED)	A1
B2	GBE0_ACT#	GBE0_MDI3-	A2
B3	LPC_FRAME#	GBE0_MDI3+	A3
B4	LPC_AD0	GBE0_LINK100#	A4
B5	LPC_AD1	GBE0_LINK1000#	A5
B6	LPC_AD2	GBE0_MDI2-	A6
B7	LPC_AD3	GBE0_MDI2+	A7
B8	LPC_DRQ0#	N/C	A8
B9	LPC_DRQ1#	GBE0_MDI1-	A9
B10	LPC_CLK	GBE0_MDI1+	A10
B11	GND (FIXED)	GND (FIXED)	A11
B12	PWRBTN#	GBE0_MDI0-	A12
B13	SMB_CK	GBE0_MDI0+	A13
B14	SMB_DAT	N/C	A14
B15	SMB_ALERT#	SUS_S3#	A15
B16	SATA1_TX+	SATA0_TX+	A16
B17	SATA1_TX-	SATA0_TX-	A17
B18	SUS_STAT#	SUS_S4#	A18
B19	SATA1_RX+	SATA0_RX+	A19
B20	SATA1_RX-	SATA0_RX-	A20
B21	GND (FIXED)	GND (FIXED)	A21
B22	SATA3_TX+	SATA2_TX+	A22
B23	SATA3_TX-	SATA2_TX-	A23
B24	PWR_OK	SUS_S5#	A24
B25	SATA3_RX+	SATA2_RX+	A25
B26	SATA3_RX-	SATA2_RX-	A26
B27	WDT	BATLOW#	A27
B28	AC_SDIN2	ATA_ACT#	A28
B29	AC_SDIN1	AC_SYNC	A29
B30	AC_SDIN0	AC_RST#	A30
B31	GND	GND	A31
B32	SPKR	AC_BITCLK	A32
B33	I2C_CK	AC_SDOUT	A33
B34	I2C_DAT	BIOS_DISABLE0#	A34
B35	THRM#	THRMTRIP#	A35
B36	USB7-	USB6-	A36
B37	USB7+	USB6+	A37
B38	USB_4_5_OC#	USB_6_7_OC#	A38
B39	USB5-	USB4-	A39
B40	USB5+	USB4+	A40
B41	GND	GND	A41
B42	USB3-	USB2-	A42
B43	USB3+	USB2+	A43
B44	USB_0_1_OC#	USB_2_3_OC#	A44
B45	USB1-	USB0-	A45
B46	USB1+	USB0+	A46
B47	EXCD1_PERST#	VCC_RTC	A47
B48	EXCD1_CPPE#	EXCD0_PERST#	A48
B49	SYS_RESET#	EXCD0_CPPE#	A49
B50	CB_RESET#	LPC_SERIRQ	A50
B51	GND	GND	A51
B52	PCIE_RX5+	PCIE_TX5+	A52
B53	PCIE_RX5-	PCIE_TX5-	A53
B54	GPO1	GPI0	A54
B55	PCIE_RX4+	PCIE_TX4+	A55

B56	PCIE_RX4-	PCIE_TX4-	A56
B57	GPO2	GND	A57
B58	PCIE_RX3+	PCIE_TX3+	A58
B59	PCIE_RX3-	PCIE_TX3-	A59
B60	GND	GND	A60
B61	PCIE_RX2+	PCIE_TX2+	A61
B62	PCIE_RX2-	PCIE_TX2-	A62
B63	GPO3	GPI1	A63
B64	PCIE_RX1+	PCIE_TX1+	A64
B65	PCIE_RX1-	PCIE_TX1-	A65
B66	WAKE0#	GND	A66
B67	WAKE1#	GPI2	A67
B68	PCIE_RX0+	PCIE_TX0+	A68
B69	PCIE_RX0-	PCIE_TX0-	A69
B70	GND	GND	A70
B71	LVDS_B0+	LVDS_A0+	A71
B72	LVDS_B0-	LVDS_A0-	A72
B73	LVDS_B1+	LVDS_A1+	A73
B74	LVDS_B1-	LVDS_A1-	A74
B75	LVDS_B2+	LVDS_A2+	A75
B76	LVDS_B2-	LVDS_A2-	A76
B77	LVDS_B3+	LVDS_VDD_EN	A77
B78	LVDS_B3-	LVDS_A3+	A78
B79	LVDS_BKLT_EN	LVDS_A3-	A79
B80	GND	GND	A80
B81	LVDS_B_CK+	LVDS_A_CK+	A81
B82	LVDS_B_CK-	LVDS_A_CK-	A82
B83	CKLVDS_BKLT_CTRL	LVDS_I2C_CK	A83
B84	VCC_5V_SBY	LVDS_I2C_DAT	A84
B85	VCC_5V_SBY	GPI3	A85
B86	VCC_5V_SBY	KBD_RST# (N/C)	A86
B87	VCC_5V_SBY	KBD_A20GATE (N/C)	A87
B88	BIOS_DIS1#	PCIE0_CK_REF+	A88
B89	VGA_RED	PCIE0_CK_REF-	A89
B90	GND	GND	A90
B91	VGA_GRN	SPI_POWER	A91
B92	VGA_BLU	SPI_MISO	A92
B93	VGA_HSYNC	GPO0	A93
B94	VGA_VSYNC	SPI_CLK	A94
B95	VGA_I2C_CK	SPI_MOSI	A95
B96	VGA_I2C_DAT	N/C	A96
B97	SPI_CS#	TYPE10#	A97
B98	N/C	N/C	A98
B99	N/C	N/C	A99
B100	GND	GND	A100
B101	FAN_PWMOUT	N/C	A101
B102	FAN_TACHIN	N/C	A102
B103	SLEEP#	LID#	A103
B104	VCC_12V	VCC_12V	A104
B105	VCC_12V	VCC_12V	A105
B106	VCC_12V	VCC_12V	A106
B107	VCC_12V	VCC_12V	A107
B108	VCC_12V	VCC_12V	A108
B109	VCC_12V	VCC_12V	A109
B110	GND	GND	A110

COM Express CD Connector (bottom side)

D1	GND (FIXED)	GND (FIXED)	C1
D2	GND	GND	C2
D3	USB_SSTX0-	USB_SSRX0-	C3
D4	USB_SSTX0+	USB_SSRX0+	C4
D5	GND	GND	C5
D6	USB_SSTX1-	USB_SSRX1-	C6
D7	USB_SSTX1+	USB_SSRX1+	C7
D8	GND	GND	C8
D9	USB_SSTX2-	USB_SSRX2-	C9
D10	USB_SSTX2+	USB_SSRX2+	C10
D11	GND (FIXED)	GND (FIXED)	C11
D12	USB_SSTX3-	USB_SSRX3-	C12
D13	USB_SSTX3+	USB_SSRX3+	C13
D14	GND	GND	C14
D15	DDI1_CTRLCLK_AUX+	DDI1_PAIR6+	C15
D16	DDI1_CTRLCLK_AUX-	DDI1_PAIR6-	C16
D17	RSVD	RSVD	C17
D18	RSVD	RSVD	C18
D19	PCIE_TX6+	PCIE_RX6+	C19
D20	PCIE_TX6-	PCIE_RX6-	C20
D21	GND(FIXED)	GND(FIXED)	C21
D22	PCIE_TX7+	PCIE_RX7+	C22
D23	PCIE_TX7-	PCIE_RX7-	C23
D24	RSVD	DDI1_HPD	C24
D25	RSVD	DDI1_PAIR4+	C25
D26	DDI1_PAIR0+	DDI1_PAIR4-	C26
D27	DDI1_PAIR0-	RSVD	C27
D28	RSVD	RSVD	C28
D29	DDI1_PAIR1+	DDI1_PAIR5+	C29
D30	DDI1_PAIR1-	DDI1_PAIR5-	C30
D31	GND(FIXED)	GND (FIXED)	C31
D32	DDI1_PAIR2+	DDI2_CTRLCLK_AUX+	C32
D33	DDI1_PAIR2-	DDI2_CTRLCLK_AUX-	C33
D34	DDI1_DDC_AUX_SEL	DDI2_DDC_AUX_SEL	C34
D35	RSVD	RSVD	C35
D36	DDI1_PAIR3+	DDI3_CTRLCLK_AUX+	C36
D37	DDI1_PAIR3-	DDI3_CTRLCLK_AUX-	C37
D38	RSVD	DDI3_DDC_AUX_SEL	C38
D39	DDI1_PAIR0+	DDI3_PAIR0+	C39
D40	DDI1_PAIR0-	DDI3_PAIR0-	C40
D41	GND(FIXED)	GND(FIXED)	C41
D42	DDI1_PAIR1+	DDI3_PAIR1+	C42
D43	DDI1_PAIR1-	DDI3_PAIR1-	C43
D44	DDI2_HPD	DDI3_HPD	C44
D45	RSVD	RSVD	C45
D46	DDI2_PAIR2+	DDI3_PAIR2+	C46
D47	DDI2_PAIR2-	DDI3_PAIR2-	C47
D48	RSVD	RSVD	C48
D49	DDI2_PAIR3+	DDI3_PAIR3+	C49
D50	DDI2_PAIR3-	DDI3_PAIR3-	C50
D51	GND (FIXED)	GND (FIXED)	C51
D52	PEG_TX0+	PEG_RX0+	C52
D53	PEG_TX0-	PEG_RX0-	C53
D54	PEG_LANE_RV#	TYPE0#	C54
D55	PEG_TX1+	PEG_RX1+	C55

D56	PEG_TX1-	PEG_RX1-	C56
D57	TYPE2#	TYPE1#	C57
D58	PEG_TX2+	PEG_RX2+	C58
D59	PEG_TX2-	PEG_RX2-	C59
D60	GND (FIXED)	GND (FIXED)	C60
D61	PEG_TX3+	PEG_RX3+	C61
D62	PEG_TX3-	PEG_RX3-	C62
D63	RSVD	RSVD	C63
D64	RSVD	RSVD	C64
D65	PEG_TX4+	PEG_RX4+	C65
D66	PEG_TX4-	PEG_RX4-	C66
D67	RSVD	RSVD	C67
D68	PEG_TX5+	PEG_RX5+	C68
D69	PEG_TX5-	PEG_RX5-	C69
D70	GND (FIXED)	GND (FIXED)	C70
D71	PEG_TX6+	PEG_RX6+	C71
D72	PEG_TX6-	PEG_RX6-	C72
D73	GND	GND	C73
D74	PEG_TX7+	PEG_RX7+	C74
D75	PEG_TX7-	PEG_RX7-	C75
D76	GND	GND	C76
D77	RSVD	RSVD	C77
D78	PEG_TX8+	PEG_RX8+	C78
D79	PEG_TX8-	PEG_RX8-	C79
D80	GND (FIXED)	GND (FIXED)	C80
D81	PEG_TX9+	PEG_RX9+	C81
D82	PEG_TX9-	PEG_RX9-	C82
D83	RSVD	RSVD	C83
D84	GND	GND	C84
D85	PEG_TX10+	PEG_RX10+	C85
D86	PEG_TX10-	PEG_RX10-	C86
D87	GND	GND	C87
D88	PEG_TX11+	PEG_RX11+	C88
D89	PEG_TX11-	PEG_RX11-	C89
D90	GND (FIXED)	GND (FIXED)	C90
D91	PEG_TX12+	PEG_RX12+	C91
D92	PEG_TX12-	PEG_RX12-	C92
D93	GND	GND	C93
D94	PEG_TX13+	PEG_RX13+	C94
D95	PEG_TX13-	PEG_RX13-	C95
D96	GND	GND	C96
D97	RSVD	RSVD	C97
D98	PEG_TX14+	PEG_RX14+	C98
D99	PEG_TX14-	PEG_RX14-	C99
D100	GND (FIXED)	GND (FIXED)	C100
D101	PEG_TX15+	PEG_RX15+	C101
D102	PEG_TX15-	PEG_RX15-	C102
D103	GND	GND	C103
D104	VCC_12V	VCC_12V	C104
D105	VCC_12V	VCC_12V	C105
D106	VCC_12V	VCC_12V	C106
D107	VCC_12V	VCC_12V	C107
D108	VCC_12V	VCC_12V	C108
D109	VCC_12V	VCC_12V	C109
D110	GND (FIXED)	GND (FIXED)	C110

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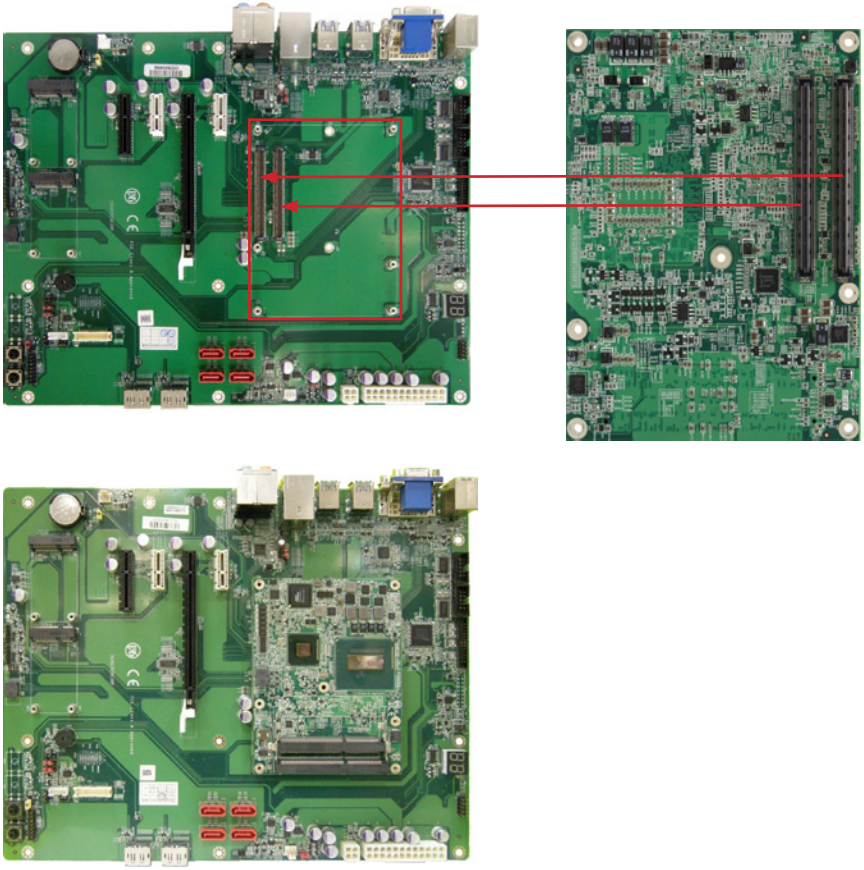
Chapter 3

Installation & Maintenance

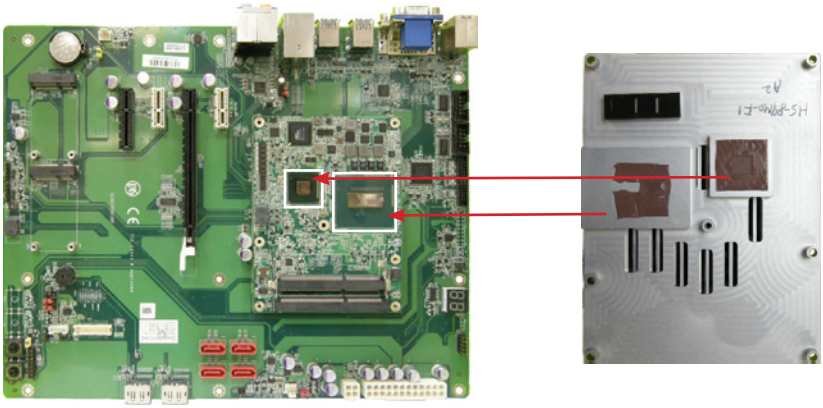
3.1 Installing the CPU Module on Carrier Board

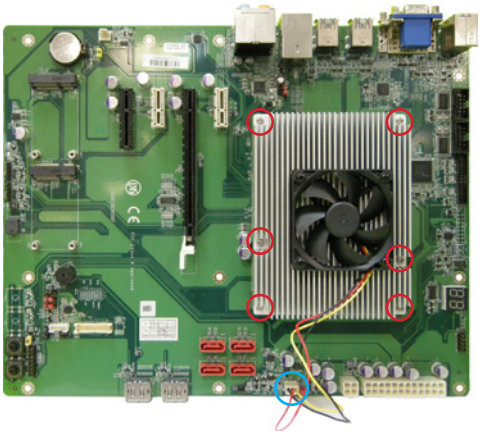
1. Find the COM Express connectors on carrier board PBE-1702, which is available in Section 1.5.1 Optional Accessories on page 4.
2. Embed EmETXe-i87M0 into PBE-1702 via COM Express connectors as below; that is, COM Express AB to AB and CD to CD.



3.2 Installing the Heatsink

1. Locate EmETXe-i87M0 mounted on PBE-1702.
2. Prepare the heatspred included in optional accessories. (See Section 1.5.1 Optional Accessories on page 4) Put heatspred on the CPU module and lock it. Make sure thermal grease in contact with CPU and chipset on CPU module. Plug power cable into appropriate connector if there is a fan.





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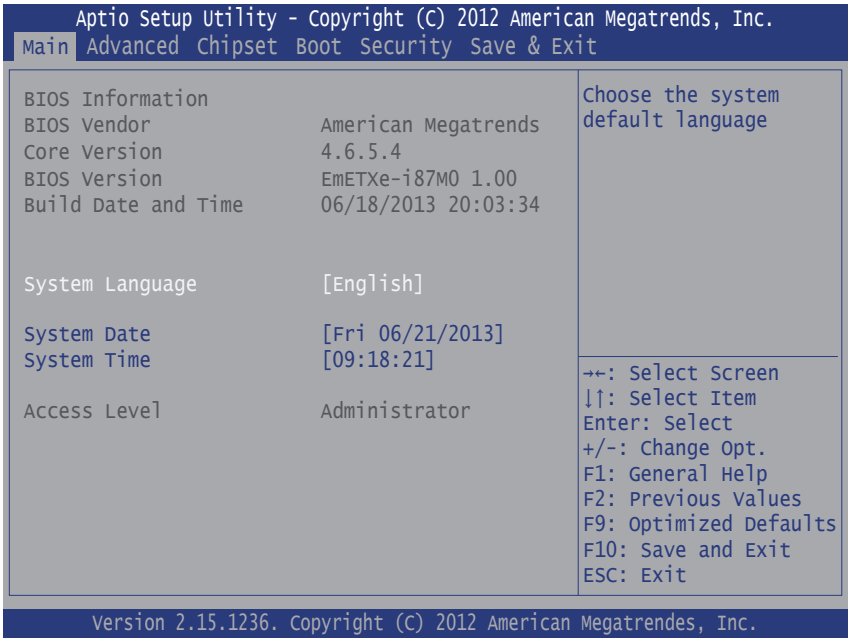
Chapter 4

BIOS

4.1 Main

The AMI BIOS provides a Setup utility program for specifying the system configurations and settings. The BIOS RAM of the system stores the Setup utility and configurations. When you turn on the computer, the AMI BIOS is immediately activated. To enter the BIOS SETUP UTILITY, press **"Delete"** once the power is turned on. When the computer is shut down, the battery on the motherboard supplies the power for BIOS RAM.

The **Main Setup** screen lists the following information:



Setting	Description
System Language	Choose the system default language.
System Date	Set the system date. Use Tab to switch between Data elements. Note that the 'Day' automatically changes when you set the date. ► The date format is: **Day:** Sun to Sat **Month:** 1 to 12 **Date:** 1 to 31 **Year:** 1998 to 2099

System Time	Set the system time. Use Tab to switch between Time elements. ► The time format is: **Hour:** 00 to 23 **Minute:** 00 to 59 **Second:** 00 to 59

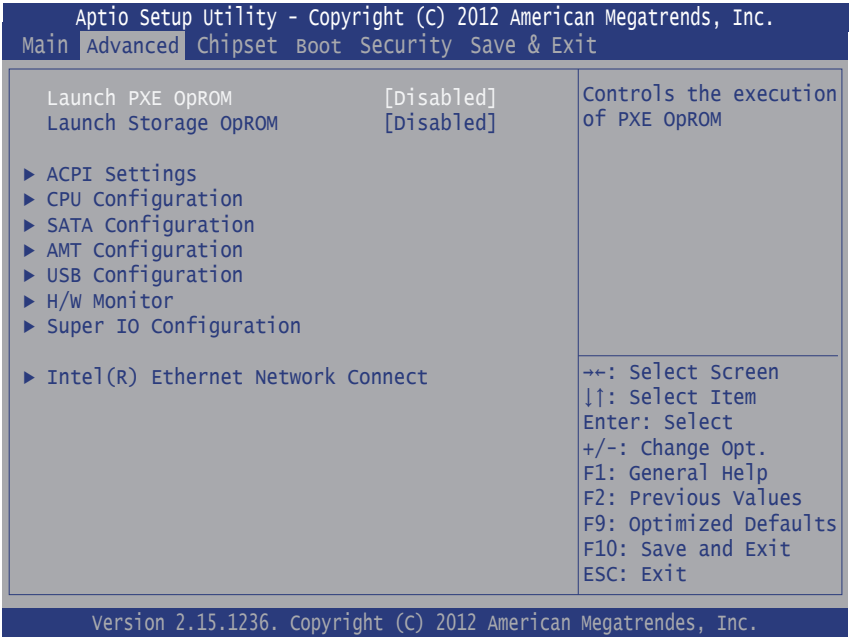
Key Commands

BIOS Setup Utility is mainly a key-based navigation interface. Please refer to the following key command instructions for navigation process.

Keystroke	Function
◄ ►	Move to highlight a particular configuration screen from the top menu bar / Move to highlight items on the screen
▼ ▲	Move to highlight previous/next item
Enter	Select and access a setup item/field
Esc	On the Main Menu – Quit the setup and not save changes into CMOS (a message screen will display and ask you to select “OK” or “Cancel” for exiting and discarding changes. Use “←” and “→” to select and press “Enter” to confirm) On the Sub Menu – Exit current page and return to main menu
Page Up / +	Increase the numeric value on a selected setup item / make change
Page Down -	Decrease the numeric value on a selected setup item / make change
F1	Activate “General Help” screen
F10	Save the changes that have been made in the setup and exit. (a message screen will display and ask you to select “OK” or “Cancel” for exiting and saving changes. Use “←” and “→” to select and press “Enter” to confirm)

4.2 Advanced

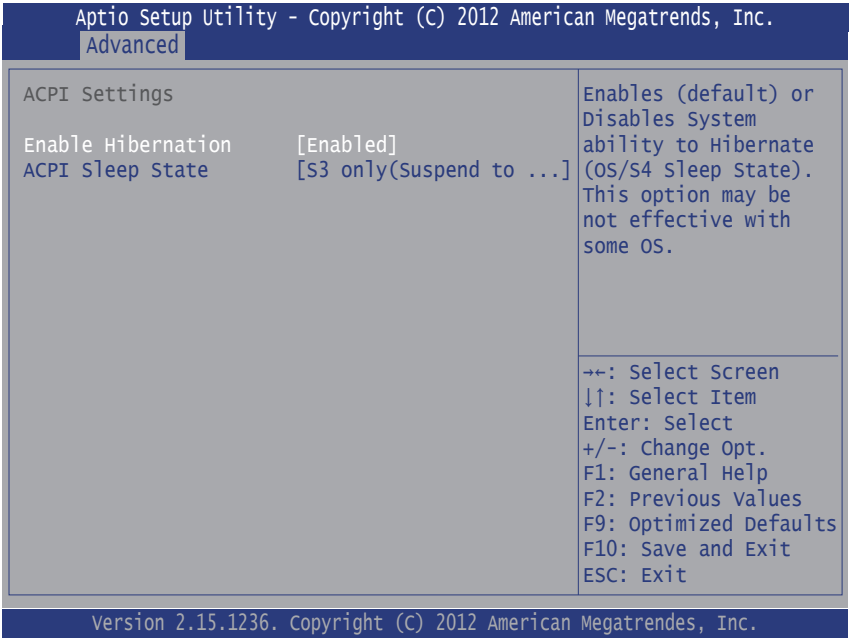
The “Advanced” setting page provides you the options to configure the details of your hardware, such as ACPI, CPU, SATA, AMT, USB and Super IO.



Setting	Description
Launch PXE OpROM	Controls the execution of PXE OpROM. ► Options: **Enabled** or **Disabled** (default)
Launch Storage OpROM	Controls the execution of Storage OpROM. ► Options: **Enabled** or **Disabled** (default)
ACPI Settings	See Section 4.2.1 ACPI Settings on page 23
CPU Configuration	See Section 4.2.2 CPU Configuration on page 24
SATA Configuration	See Section 4.2.3 SATA Configuration on page 25
AMT Configuration	See Section 4.2.4 AMT Configuration on page 26
USB Configuration	See Section 4.2.5 USB Configuration on page 27

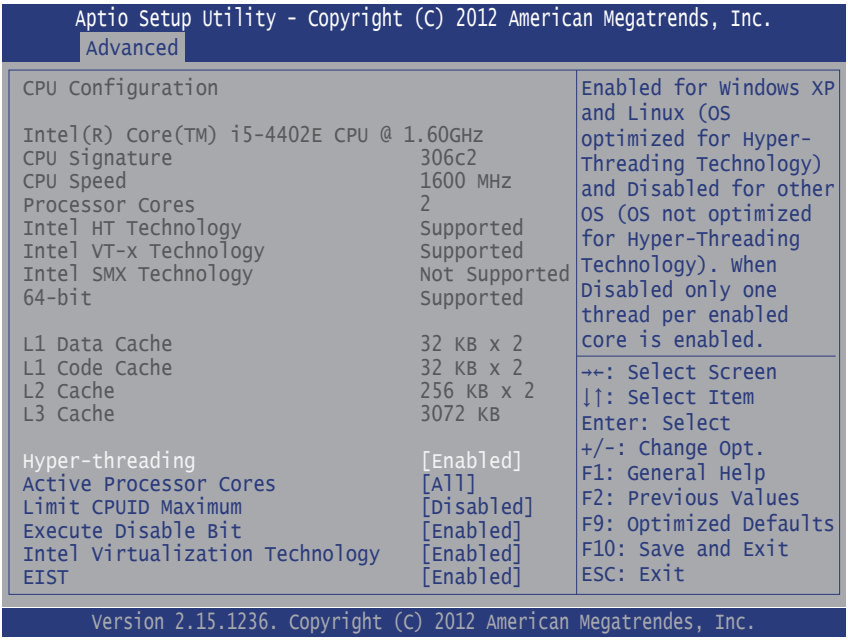
H/W Monitor	See Section 4.2.6 H/W Monitor on page 28
Super IO Configuration	See Section 4.2.7 Super IO Configuration on page 29
Intel(R) Ethernet Network Connect	See Section 4.2.8 Intel(R) Ethernet Network Connect on page 31

4.2.1 ACPI Settings



Setting	Description
Enable Hibernation	**Enables** (default) or **Disables** System ability to Hibernate (OS/S4 Sleep State). This option may be not effective with some OS.
ACPI Sleep State	Select ACPI sleep state the system will enter when the SUSPEND button is pressed. ► Options: **Suspend Disabled**, **S1 only(CPU Stop Clock)**, **S3 only(Suspend to RAM)** (default), **Both S1 and S3 available for OS to choose from**

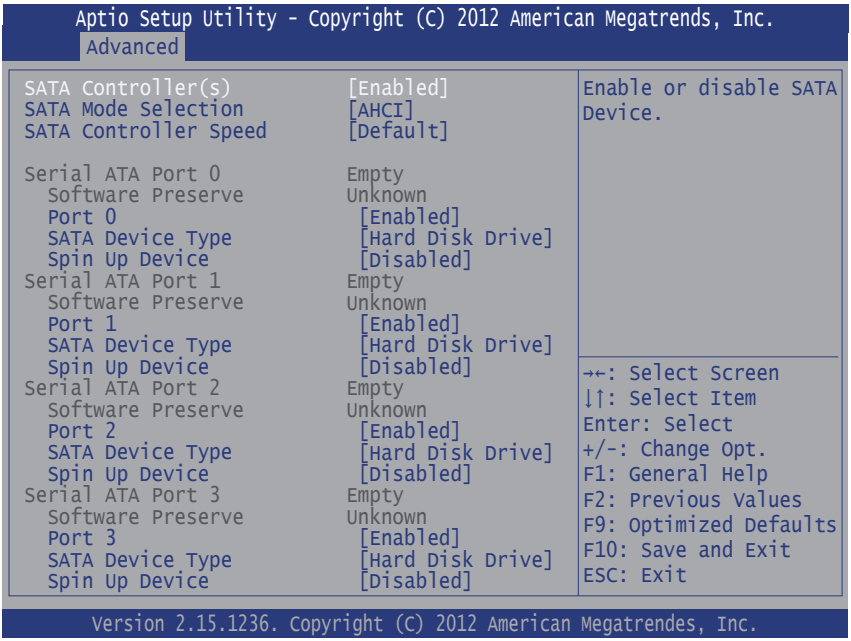
4.2.2 CPU Configuration



Setting	Description
Hyper-threading	**Enabled** (default) for Windows XP and Linux (OS optimized for Hyper-Threading Technology) and **Disabled** for other OS (OS not optimized or Hyper-Threading Technology). When Disabled only one thread per enabled core is enabled.
Active Processor Cores	Number of cores to enable in each processor package. ► Options: **All** (default) and **1**
Limit CPUID Maximum	Disabled for Windows XP ► Options: **Enabled** or **Disabled** (default)
Execute Disable Bit	XD can prevent certain classes of malicious buffer overflow attacks when combined with a supporting OS (Windows Server 2003 SP1, Windows XP SP2, SuSE Linux 9.2, RedHat Enterprise 3 Update 3.) ► Options: **Enabled** (default) or **Disabled**

Intel Virtualization Technology	When enabled, a VMM can utilize the additional hardware capabilities provided by Vanderpool Technology ► Options: **Enabled** (default) or **Disabled**
EIST	**Enable** (default)/**Disable** Intel SpeedStep

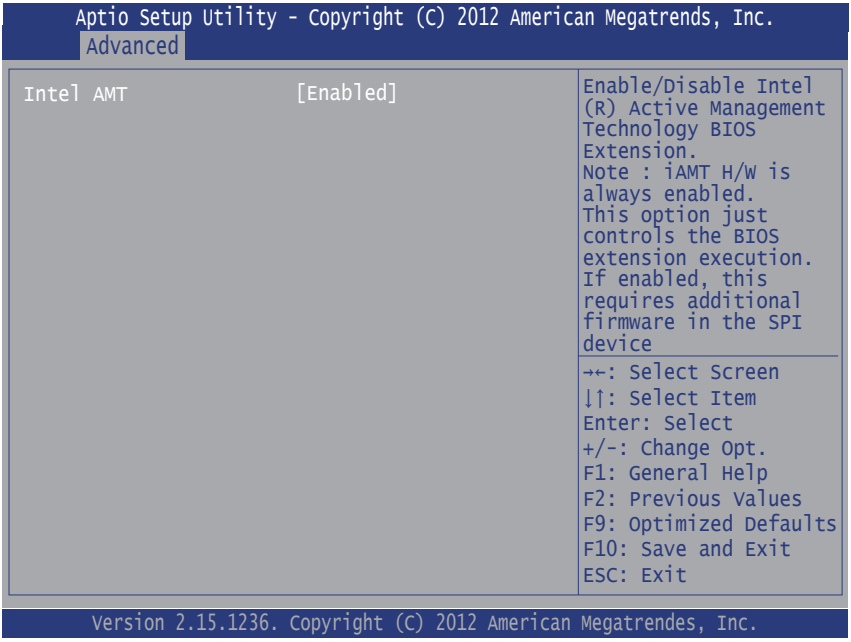
4.2.3 SATA Configuration



Setting	Description
SATA Controller(s)	**Enable** (default) or **disable** SATA Device.
SATA Mode Selection	Determines how SATA controller(s) operate. ► Options: **IDE**, **AHCI** (default) or **RAID**
SATA Controller Speed	Indicates the maximum speed the SATA controller can support. ► Options: **Default** (default), **Gen1**, **Gen2**, **Gen3**
Port 0/1/2/3	**Enable** (default) or **disable** SATA Port.

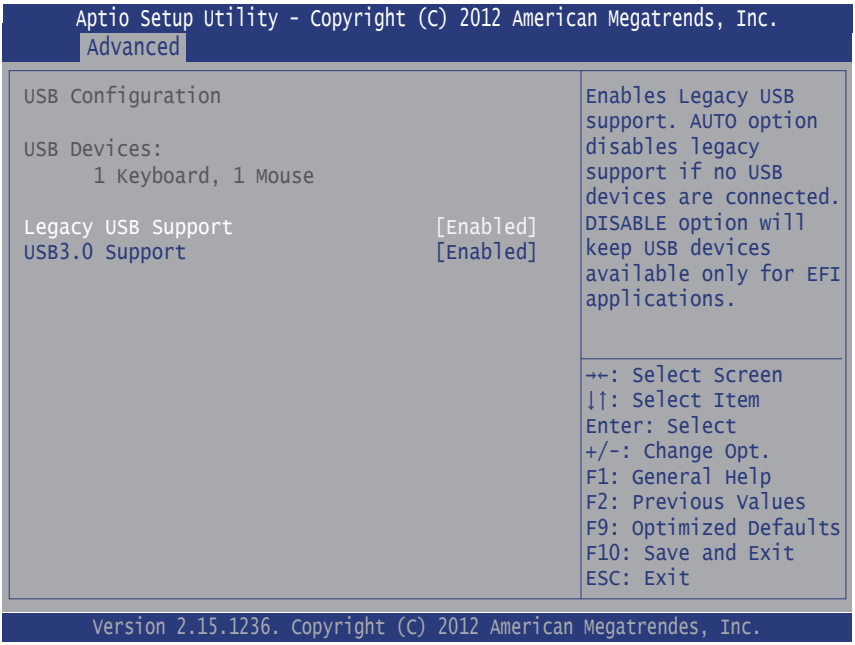
SATA Device Type	Identify the SATA port is connected to **Solid State Drive** or **Hard Disk Drive** (default).
Spin Up Device	On an edge detect from 0 to 1, the PCH starts a COMRESET initialization sequence to the device. ► Options: **Enabled** or **Disabled** (default)

4.2.4 AMT Configuration



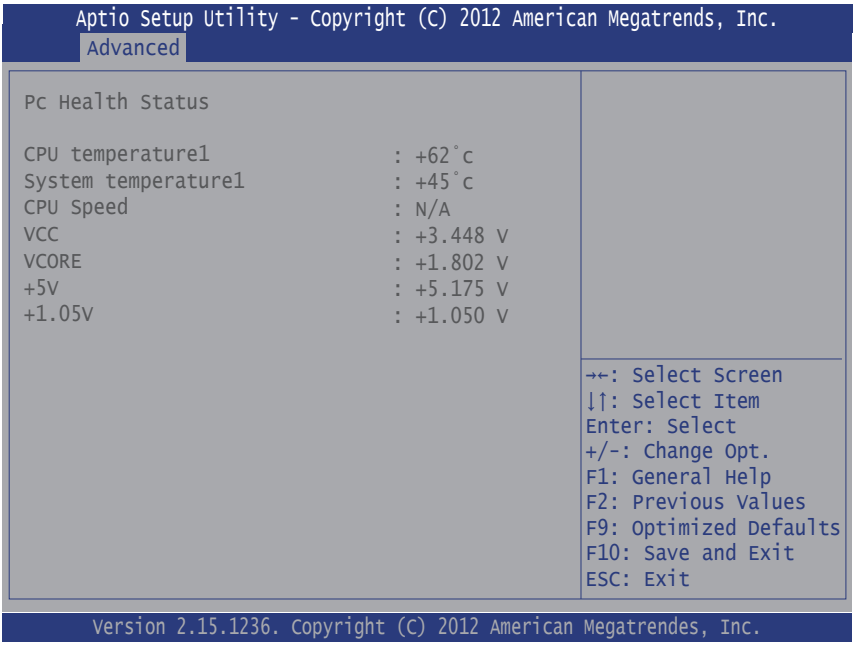
Setting	Description
Intel AMT	**Enable** (default)/**Disable** Intel(R) Active Management Technology BIOS Extension. Note : iAMT H/W is always enabled. This option just controls the BIOS extension execution. If enabled, this requires additional firmware in the SPI device.

4.2.5 USB Configuration

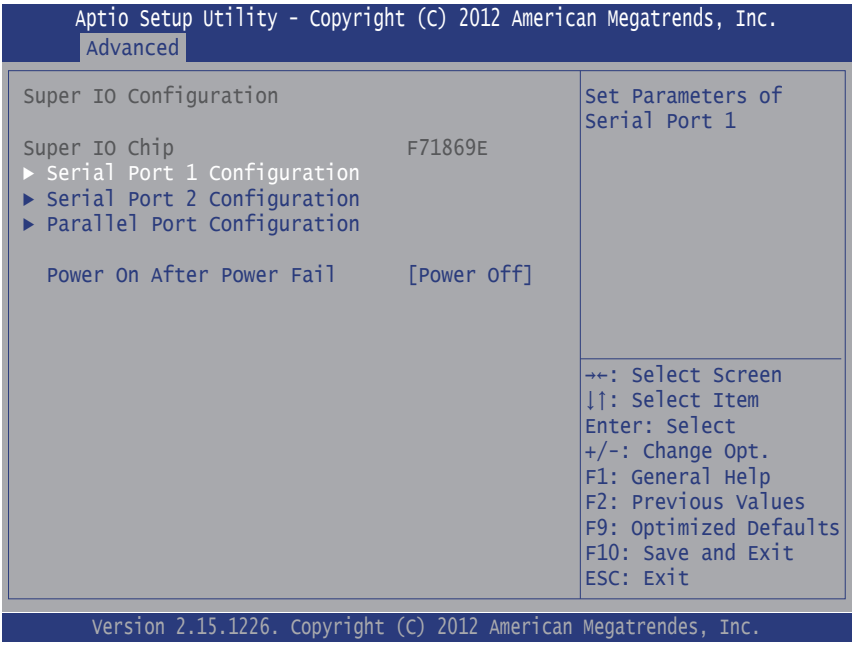


Setting	Description
Legacy USB Support	**Enables** (default) Legacy USB support. **AUTO** option disables legacy support if no USB devices are connected. **DISABLE** option will keep USB devices available only for EFI applications.
USB3.0 Support	**Enable** (default)/**Disable** USB3.0 (XHCI) Controller support.

4.2.6 H/W Monitor

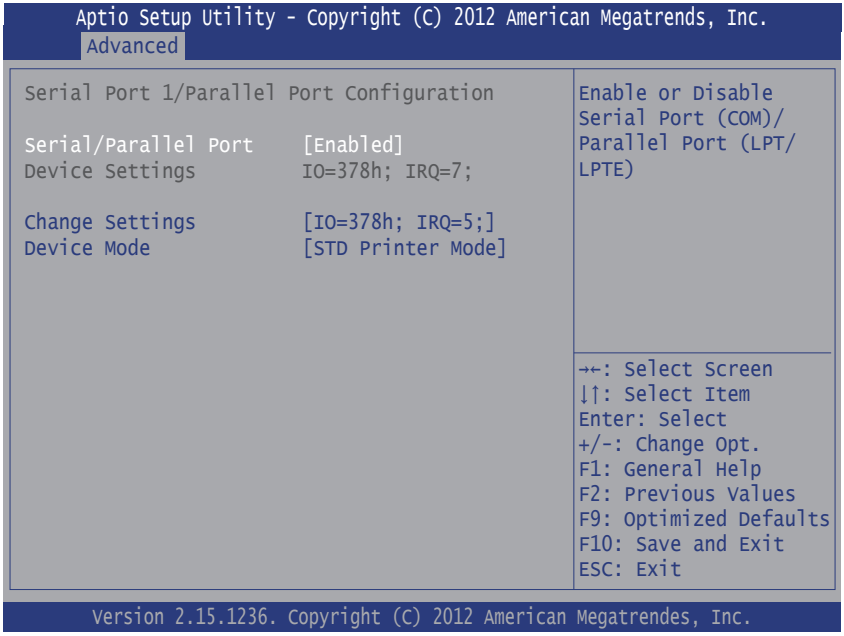


4.2.7 Super IO Configuration



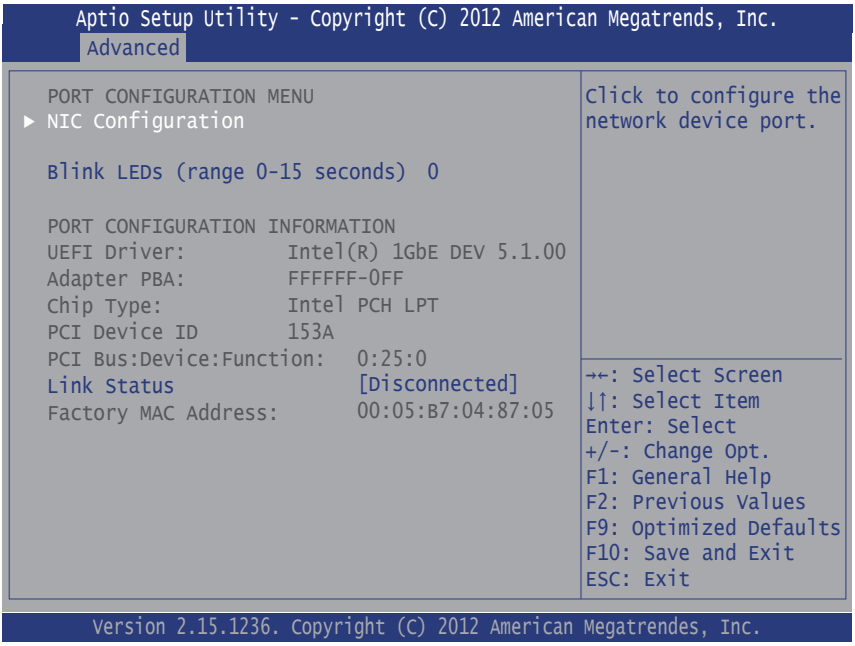
Setting	Description
Serial Port 1 Configuration	See next page.
Serial Port 2 Configuration	
Parallel Port Configuration	
Power On After Power Fail	Specify what state to go to when power is re-applied after a power failure. ► Options: **Last State**, **Power On** and **Power Off** (default)

Serial Port 1~2/ Parallel Port Configuration



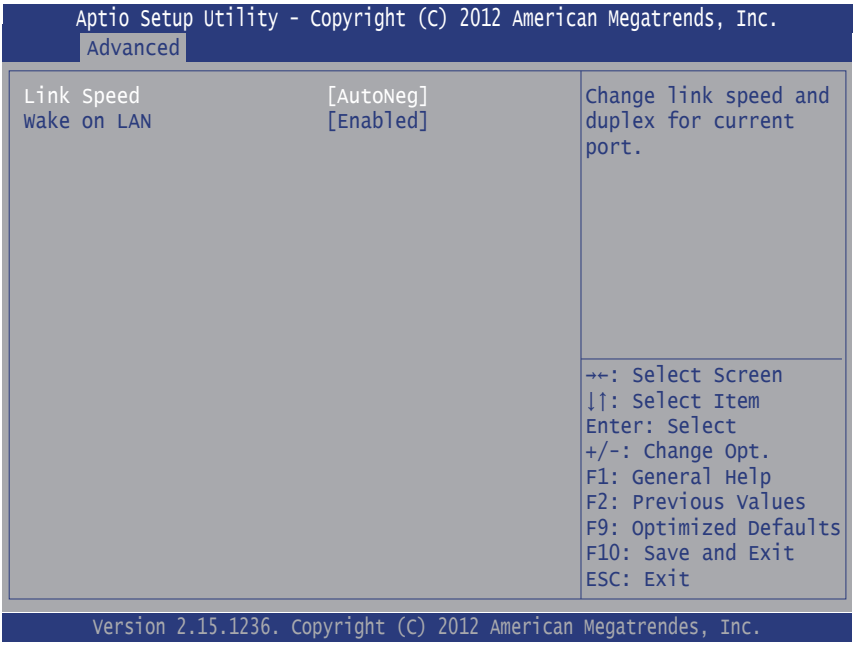
Setting	Description
Serial Port	**Enable** (default) or **Disable** Serial Port (COM).
Parallel Port	**Enable** (default) or **Disable** Parallel Port (LPT/LPTE).
Change Settings	Select an optimal setting for Super IO device. ► Options: **IO=3F8h; IRQ=4** (default for Serial Port 1); **IO=2F8h; IRQ=3** (default for Serial Port 2); **IO=378h; IRQ=5** (default for Parallel Port); **Auto**; **IO=378h; IRQ=5, 6, 7, 9, 10, 11, 12**; **IO=278h; IRQ=5, 6, 7, 9, 10, 11, 12**; **IO=3BCh; IRQ=5, 6, 7, 9, 10, 11, 12**;
Device Mode (only for Parallel Port Configuration)	Change the Printer Port mode. ► Options: **STD Printer Mode** (default), **SPP Mode**, **EPP-1.9 and SPP Mode**, **EPP-1.7 and SPP Mode**, **ECP Mode**, **ECP and EPP 1.9 Mode**, **ECP and EPP 1.7 Mode**.

4.2.8 Intel(R) Ethernet Network Connect



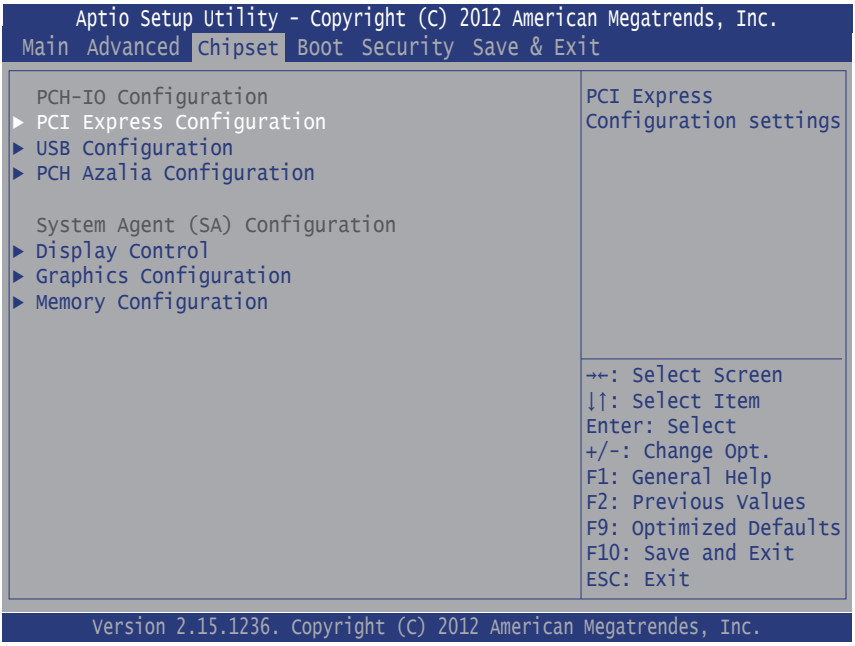
Setting	Description
NIC Configuration	See next page.
Blink LEDs (range 0-15 seconds)	Blink LEDs for the specified duration (up to 15 seconds).
Link Status	Link Status

NIC Configuration



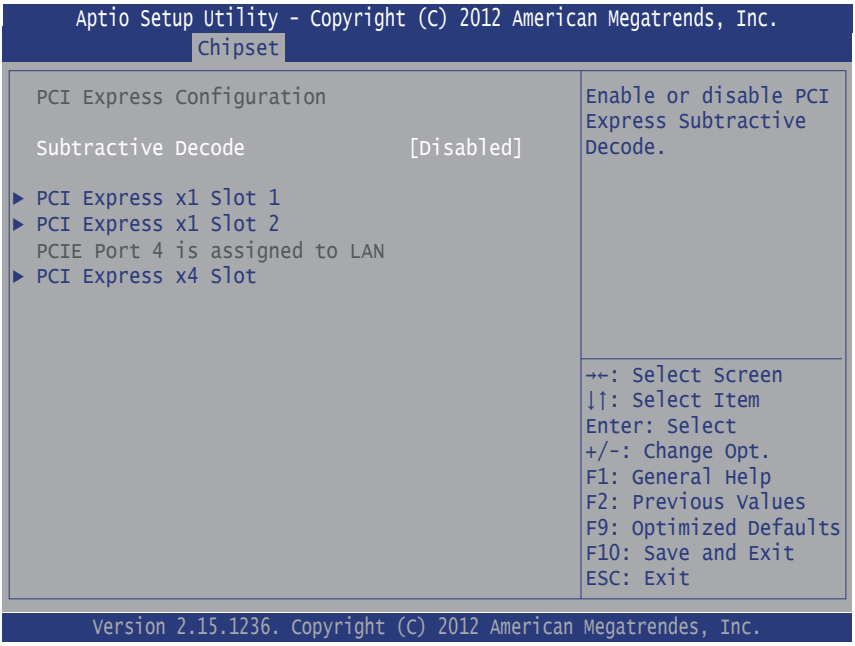
Setting	Description
Link Speed	Change link speed and duplex for current port. ► Options: **AutoNeg** (default), **10 Mbps Half**, **10 Mbps Full**, **100 Mbps Half**, **100 Mbps Full**
Wake on LAN	Enable this option to wake the system with a magic packet. ► Options: **Enabled** (default) or **Disabled**

4.3 Chipset



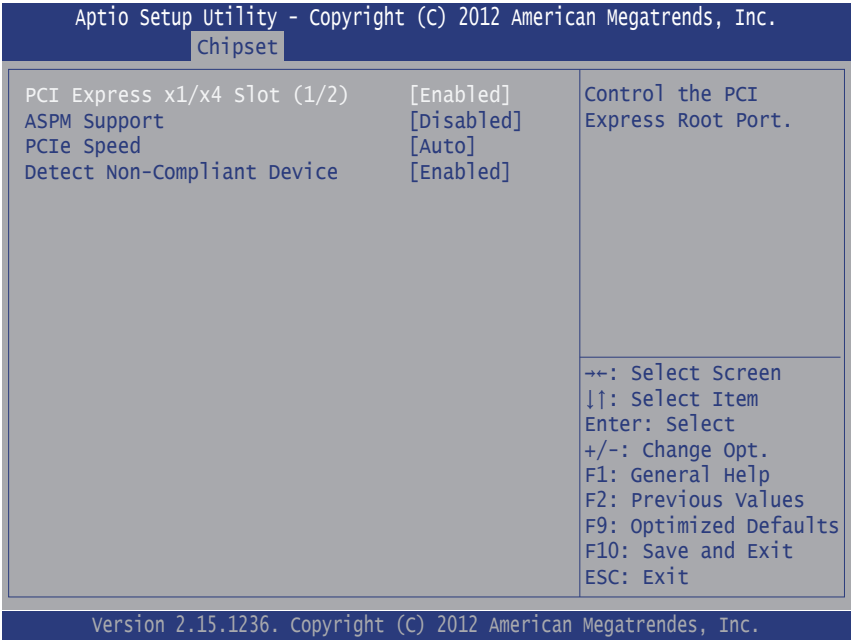
Setting	Description
PCI Express Configuration	See Section 4.3.1 PCI Express Configuration on page 34
USB Configuration	See Section 4.3.2 USB Configuration on page 36
PCH Azalia Configuration	See Section 4.3.3 PCH Azalia Configuration on page 37
Display Control	See Section 4.3.4 Display Control on page 38
Graphics Configuration	See Section 4.3.5 Graphics Configuration on page 39
Memory Configuration	See Section 4.3.6 Memory Configuration on page 40

4.3.1 PCI Express Configuration



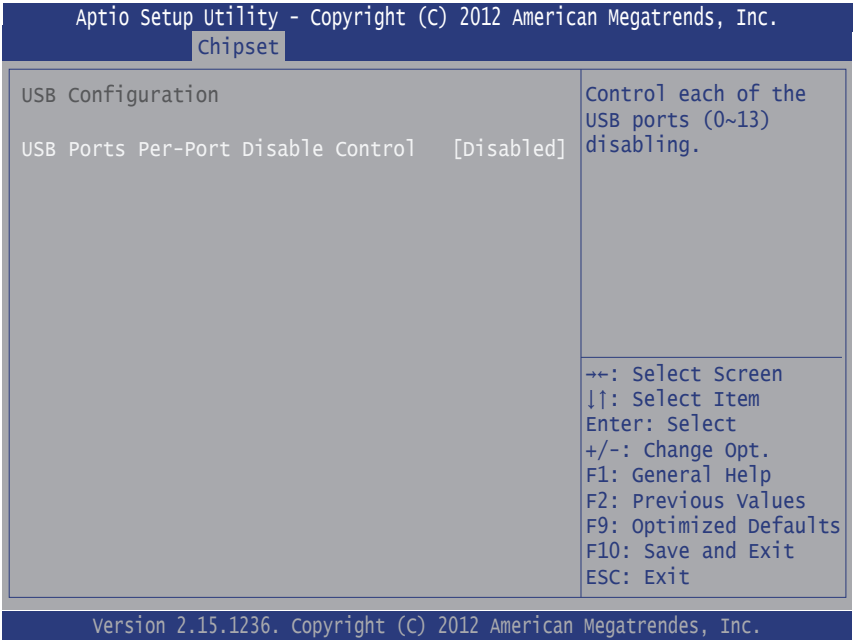
Setting	Description
Subtractive Decode	**Enable** or **disable** (default) PCI Express Subtractive Decode.
PCI Express x1 Slot 1	See next page.
PCI Express x1 Slot 2	
PCI Express x4 Slot	

PCI Express x1/x4 Slot (1/2)



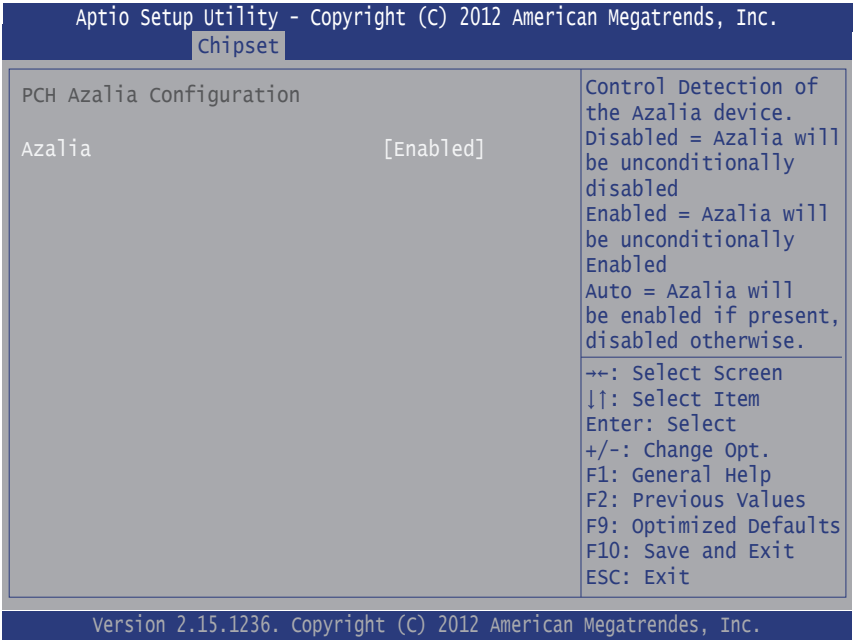
Setting	Description
PCI Express x1 Slot 1 PCI Express x1 Slot 2 PCI Express x4 Slot	Control the PCI Express Root Port. ► Options: **Enabled** (default) or **Disabled**
ASPM Support	Set the ASPM Level: Force L0s - Force all links to L0s State: Auto - BIOS auto configure: DISABLE - Disable ASPM ► Options: **Disabled** (default), **L0s**, **L1**, **L0sL1** and **Auto**
PCIe Speed	Select PCI Express port speed. ► Options: **Auto** (default), **Gen1** and **Gen2**
Detect Non-Compliant Device	Detect Non-Compliance PCI Express Device. If enabled, it will take more time at POST time. ► Options: **Enabled** (default) or **Disabled**

4.3.2 USB Configuration



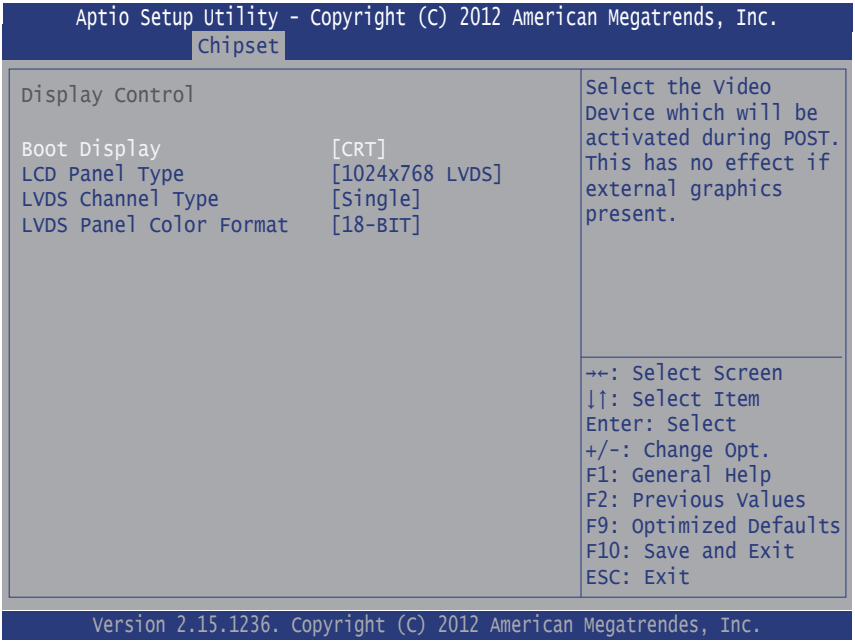
Setting	Description
USB Ports Per-Port Disable Control	Control each of the USB ports (0~13) disabling. ► Options: **Enabled** or **Disabled** (default)

4.3.3 PCH Azalia Configuration



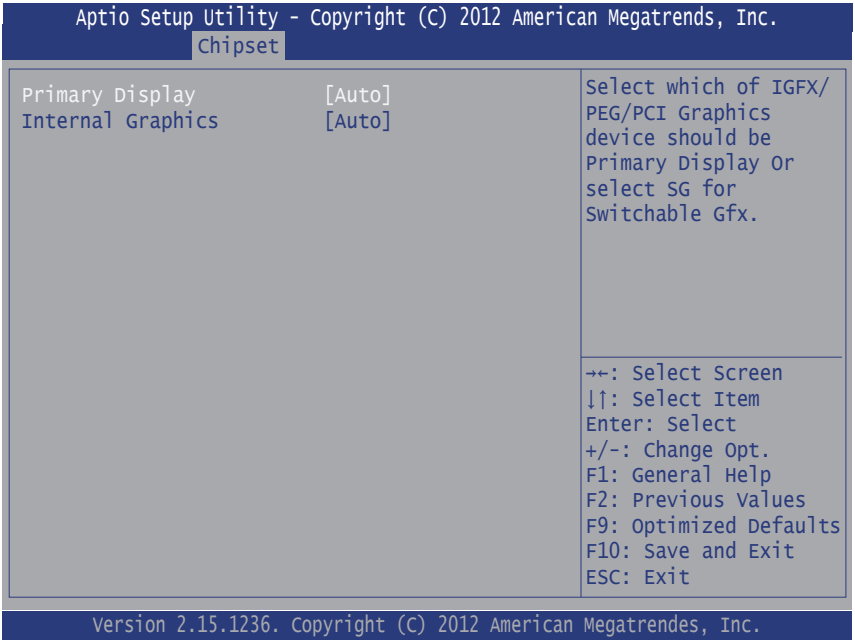
Setting	Description
Azalia	Control Detection of the Azalia device. **Disabled** = Azalia will be unconditionally disabled **Enabled** (default) = Azalia will be unconditionally Enabled **Auto** = Azalia will be enabled if present, disabled otherwise.

4.3.4 Display Control



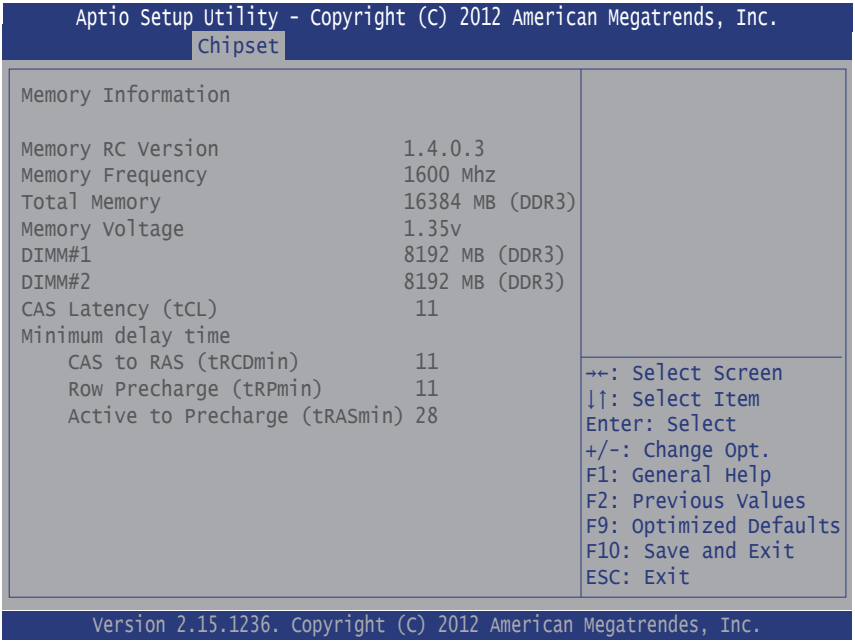
Setting	Description
Boot Display	Select the Video Device which will be activated during POST. This has no effect if external graphics present. ► Options: **CRT** (default), **LVDS**, **DVI**, **DigitalPort1** and **DigitalPort2**
LCD Panel Type	Select LCD panel used by Internal Graphics Device by selecting the appropriate setup item. ► Options: **VBIOS Default**, **640x480/800x600/1024x768** (default)/**1280x1024/1400x1050/1600x1200/1366x768/1680x1050/1920x1200/1440x900/1600x900/1024x768/1280x800/1920x1080/2048x1536 LVDS**
LVDS Channel Type	Select **single** (default) or **dual** channel
LVDS Panel Color Format	Select LVDS color display mode ► Options: **24-BIT** or **18-BIT** (default)

4.3.5 Graphics Configuration

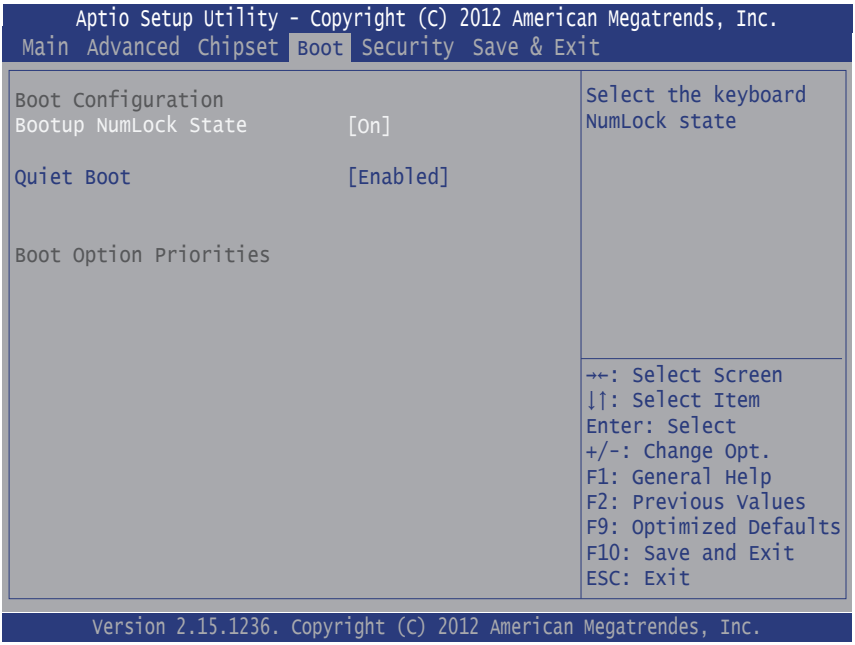


Setting	Description
Primary Display	Select which of IGFX/PEG/PCI Graphics device should be Primary Display Or select SG for Switchable Gfx. ► Options: **Auto** (default), **IGFX**, **PEG** and **PCIE**
Internal Graphics	Keep IGD enabled based on the setup options. ► Options: **Auto** (default), **Disabled** and **Enabled**

4.3.6 Memory Configuration



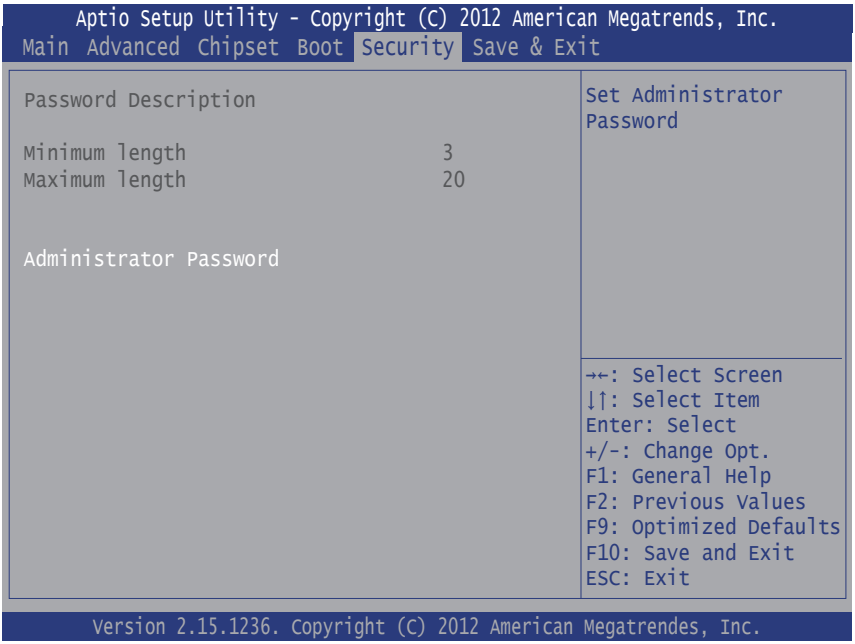
4.4 Boot



Setting	Description
Boot NumLock State	Select the keyboard NumLock state. ► Options: **On** (default) and **Off**.
Quiet Boot	**Enables** (default) or **Disables** Quiet Boot option.

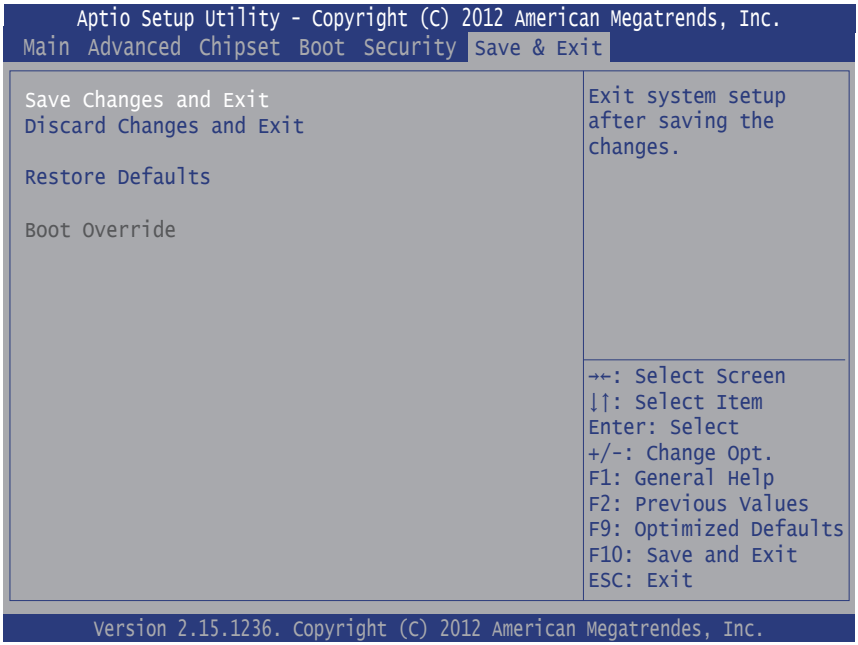
4.5 Security

The **Security** menu sets up the administrator password.



Setting	Description
Administrator Password	To set up an administrator password: 1. Select **Administrator Password**. The screen then pops up an **Create New Password** dialog. 2. Enter your desired password that is no less than 3 characters and no more than 20 characters. 3. Hit [Enter] key to submit.

4.6 Save & Exit



Setting	Description
Save Changes and Exit	Exit system setup after saving the changes. ► Enter the item and then a dialog box pops up: **Save configuration and exit? (Yes/ No)**
Discard Changes and Exit	Exit system setup without saving the changes. ► Enter the item and then a dialog box pops up: **Quit without saving? (Yes/ No)**
Restore Defaults	Restore/Load Default values for all the setup options. ► Enter the item and then a dialog box pops up: **Load Optimized Defaults? (Yes/ No)**

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Appendix

Appendix A: I/O Port Address Map

Each peripheral device in the system is assigned a set of I/O port addresses which also becomes the identity of the device. The following table lists the I/O port addresses used.

Address	Device Description
0x00001854-0x00001857	Motherboard resources
0x00000020-0x00000021	Programmable interrupt controller
0x00000024-0x00000025	Programmable interrupt controller
0x00000028-0x00000029	Programmable interrupt controller
0x0000002C-0x0000002D	Programmable interrupt controller
0x00000030-0x00000031	Programmable interrupt controller
0x00000034-0x00000035	Programmable interrupt controller
0x00000038-0x00000039	Programmable interrupt controller
0x0000003C-0x0000003D	Programmable interrupt controller
0x000000A0-0x000000A1	Programmable interrupt controller
0x000000A4-0x000000A5	Programmable interrupt controller
0x000000A8-0x000000A9	Programmable interrupt controller
0x000000AC-0x000000AD	Programmable interrupt controller
0x000000B0-0x000000B1	Programmable interrupt controller
0x000000B4-0x000000B5	Programmable interrupt controller
0x000000B8-0x000000B9	Programmable interrupt controller
0x000000BC-0x000000BD	Programmable interrupt controller
0x000004D0-0x000004D1	Programmable interrupt controller
0x000004D0-0x000004D1	Motherboard resources
0x00000040-0x00000043	System timer
0x00000050-0x00000053	System timer
0x0000F000-0x0000F03F	Intel(R) HD Graphics 4600
0x000003B0-0x000003BB	Intel(R) HD Graphics 4600
0x000003C0-0x000003DF	Intel(R) HD Graphics 4600
0x00000000-0x0000001F	Direct memory access controller
0x00000000-0x0000001F	PCI bus
0x00000081-0x00000091	Direct memory access controller

0x00000093-0x0000009F	Direct memory access controller
0x000000C0-0x000000DF	Direct memory access controller
0x0000F040-0x0000F05F	Intel(R) 8 Series/C220 Series SMBus Controller - 8C22
0x00000060-0x00000060	Standard PS / 2 Keyboard
0x00000064-0x00000064	Standard PS / 2 Keyboard
0x00000378-0x0000037F	Printer Port (LPT1)
0x000003F8-0x000003FF	Communications Port (COM1)
0x000002F8-0x000002FF	Communications Port (COM2)
0x00000D00-0x0000FFFF	PCI bus
0x00000070-0x00000077	System CMOS/real time clock
0x00000070-0x00000077	Motherboard resources
0x00000010-0x0000001F	Motherboard resources
0x00000022-0x0000003F	Motherboard resources
0x00000044-0x0000005F	Motherboard resources
0x00000072-0x0000007F	Motherboard resources
0x00000080-0x00000080	Motherboard resources
0x00000080-0x00000080	Motherboard resources
0x00000084-0x00000086	Motherboard resources
0x00000088-0x00000088	Motherboard resources
0x0000008C-0x0000008E	Motherboard resources
0x00000090-0x0000009F	Motherboard resources
0x000000A2-0x000000BF	Motherboard resources
0x000000E0-0x000000EF	Motherboard resources
0x00000A00-0x00000A1F	Motherboard resources
0x00000290-0x0000029F	Motherboard resources
0x0000002E-0x0000002F	Motherboard resources
0x0000004E-0x0000004F	Motherboard resources
0x00000061-0x00000061	Motherboard resources
0x00000063-0x00000063	Motherboard resources
0x00000065-0x00000065	Motherboard resources
0x00000067-0x00000067	Motherboard resources

0x00000092-0x00000092	Motherboard resources
0x000000B2-0x000000B3	Motherboard resources
0x00000680-0x0000069F	Motherboard resources
0x0000FFFF-0x0000FFFF	Motherboard resources
0x0000FFFF-0x0000FFFF	Motherboard resources
0x0000FFFF-0x0000FFFF	Motherboard resources
0x00001C00-0x00001CFE	Motherboard resources
0x00001D00-0x00001DFE	Motherboard resources
0x00001E00-0x00001EFE	Motherboard resources
0x00001F00-0x00001FFE	Motherboard resources
0x00001800-0x000018FE	Motherboard resources
0x0000164E-0x0000164F	Motherboard resources
0x0000F0D0-0x0000F0D7	Intel(R) 8 Series SATA AHCI Controller - 8C03
0x0000F0C0-0x0000F0C3	Intel(R) 8 Series SATA AHCI Controller - 8C03
0x0000F0B0-0x0000F0B7	Intel(R) 8 Series SATA AHCI Controller - 8C03
0x0000F0A0-0x0000F0A3	Intel(R) 8 Series SATA AHCI Controller - 8C03
0x0000F060-0x0000F07F	Intel(R) 8 Series SATA AHCI Controller - 8C03
0x000000F0-0x000000F0	Numeric data processor
0x0000F0E0-0x0000F0E7	Intel(R) Active Management Technology - SOL (COM3)

Appendix B: BIOS Memory Mapping

Address	Device Description
0xFF000000-0xFFFFFFFF	Intel(R) 82802 Firmware Hub Device
0xFF000000-0xFFFFFFFF	Motherboard resources
0xF7C00000-0xF7CFFFFF	Intel(R) 8 Series/C220 Series PCI Express Root Port #3 - 8C14
0xF7C00000-0xF7CFFFFF	PCI standard PCI-to-PCI bridge
0xF7D30000-0xF7D33FFF	High Definition Audio Controller
0xFED00000-0xFED003FF	High Precision Event Timer, HPET
0xF7800000-0xF7BFFFFF	Intel(R) HD Graphics 4600
0xE0000000-0xEFFFFFFF	Intel(R) HD Graphics 4600
0xA0000-0xBFFFF	Intel(R) HD Graphics 4600
0xA0000-0xBFFFF	PCI bus
0xF7D39000-0xF7D390FF	Intel(R) 8 Series/C220 Series SMBus Controller - 8C22
0xF7D3B000-0xF7D3B3FF	Intel(R) 8 Series/C220 Series USB Enhanced Host Controller #1 - 8C26
0xD0000-0xD3FFF	PCI bus
0xD4000-0xD7FFF	PCI bus
0xD8000-0xDBFFF	PCI bus
0xDC000-0xDFFFF	PCI bus
0xE0000-0xE3FFF	PCI bus
0xE4000-0xE7FFF	PCI bus
0xDF200000-0xFEAFFFFF	PCI bus
0xF7D34000-0xF7D37FFF	High Definition Audio Controller
0xF7D3C000-0xF7D3C3FF	Intel(R) 8 Series/C220 Series USB Enhanced Host Controller #2 - 8C2D
0xFED40000-0xFED44FFF	System board
0xFED1C000-0xFED1FFFF	Motherboard resources
0xFED10000-0xFED17FFF	Motherboard resources
0xFED18000-0xFED18FFF	Motherboard resources
0xFED19000-0xFED19FFF	Motherboard resources

0xF8000000-0xFBFFFFFF	Motherboard resources
0xFED20000-0xFED3FFFF	Motherboard resources
0xFED90000-0xFED93FFF	Motherboard resources
0xFED45000-0xFED8FFFF	Motherboard resources
0xFEE00000-0xFEEFFFFF	Motherboard resources
0xF7FEF000-0xF7FEFFFF	Motherboard resources
0xF7FF0000-0xF7FF0FFF	Motherboard resources
0xF7D00000-0xF7D1FFFF	Intel(R) Ethernet Connection I217-LM
0xF7D3D000-0xF7D3DFFF	Intel(R) Ethernet Connection I217-LM
0xF7D20000-0xF7D2FFFF	Intel (R) USB 3.0 Extensible Host Controller
0xF7D3A000-0xF7D3A7FF	Intel(R) 8 Series SATA AHCI Controller - 8C03
0xF7D40000-0xF7D4000F	Intel(R) Management Engine Interface
0xF7D3E000-0xF7D3EFFF	Intel(R) Active Management Technology - SOL (COM3)

Appendix C: Interrupt Request Lines (IRQ)

Peripheral devices use interrupt request lines to notify CPU for the service required. The following table shows the IRQ used by the devices on board.

Level	Function
IRQ 0	System timer
IRQ 1	Standard PS / 2 Keyboard
IRQ 3	Communications Port (COM2)
IRQ 4	Communications Port (COM1)
IRQ 8	System CMOS/real time clock
IRQ 10	Intel(R) 8 Series/C220 Series SMBus Controller - 8C22
IRQ 12	Microsoft PS/2 Mouse
IRQ 13	Numeric data processor

Appendix D: Watchdog Timer (WDT) Setting

WDT is widely used for industry application to monitor the activity of CPU. Application software depends on its requirement to trigger WDT with adequate timer setting. Before WDT time out, the functional normal system will reload the WDT. The WDT never time out for a normal system. The WDT will not be reloaded by an abnormal system, then WDT will time out and reset the system automatically to avoid abnormal operation.

This board supports 255 levels watchdog timer by software programming I/O ports. Below are the source codes written in C, please take them as WDT application example.

```
/*-----  Include Header Area -----*/
#include "math.h"
#include "stdio.h"
#include "dos.h"

#define   DELAY_TIME                          10

int SMB_PORT_AD    = 0xF040;
int SMB_DEVICE_ADD = 0x6e; /* 75111R's Add=6eh */

unsigned char     WDTCount;

void WDT_Start(void);
int  WDT_Count(void);
unsigned char SMB_Byte_READ(int SMPORT, int DeviceID, int iREG_INDEX);
void SMB_Byte_WRITE(int SMPORT, int DeviceID, int oREG_INDEX, int oREG_DATA);

/*-----  routing, sub-routing -----*/
void main()
{
         unsigned char     iCount;

         printf("WDT Times ( 1 ~ 127 ) : \0");
         scanf("%d",&WDTCount);
         printf("\n");

         WDT_Start();

         while(1)
         {
                  iCount = WDT_Count();
                  printf("\r Counts : %d ",iCount);

                  delay(100000);
         }
}

void WDT_Start(void)
{
         unsigned char bData;
```

```
        /* Configuration and Control Register - Enable WDTOUT10# output */
        bData = SMB_Byte_READ(SMB_PORT_AD,SMB_DEVICE_ADD,0x01);
        bData = bData | 0x20;
        SMB_Byte_WRITE(SMB_PORT_AD,SMB_DEVICE_ADD,0x01,bData);
        delay(DELAY_TIME);

        /* Watchdog Timer Control Register */
        SMB_Byte_WRITE(SMB_PORT_AD,SMB_DEVICE_ADD,0x36,0x28);
        delay(DELAY_TIME);

        /* WDTOUT10 Control Register - Enable WDTOUT10 Output Timer */
        SMB_Byte_WRITE(SMB_PORT_AD,SMB_DEVICE_ADD,0x35,(0x80|WDTCount));

}

int WDT_Count(void)
{
    unsigned char bData;

        bData = SMB_Byte_READ(SMB_PORT_AD,SMB_DEVICE_ADD,0x35) & 0xFF7F;

    return bData;
}

unsigned char SMB_Byte_READ(int SMPORT, int DeviceID, int iREG_INDEX)
{
        unsigned char iData;
        unsigned char iFlag;
        int iError = 0;

        do
        {
                outportb(SMPORT+00, 0x1E);
                iFlag = inportb(SMPORT+00);
                if( iError++ > 0x8000 )    return 2;
        }
        while( ( iFlag & 0x9F ) != 0 );

        outportb(SMPORT+04, DeviceID+1);
        outportb(SMPORT+03, iREG_INDEX);
        outportb(SMPORT+02, 0x48);

        iError = 0;
        do
        {
                if( iError++ > 0x8000)     return 2;
                if( ( inportb(SMPORT+0x00) & 0x06 ) == 0x06 )        return 1;
        }
        while( (inportb(SMPORT+0x00) & 0x06 ) != 0x02 );

        iData = inportb(SMPORT+05);

        return iData;
}
```

```
void SMB_Byte_WRITE(int SMPORT, int DeviceID, int oREG_INDEX, int oREG_DATA)
{
        unsigned char iFlag;
        int iError = 0;

        do
        {
                outportb(SMPORT+00, 0x1E);
                iFlag = inportb(SMPORT+00);
                if( iError++ > 0x8000 )    return;
        }
        while( ( iFlag & 0x9F ) != 0 );

        outportb(SMPORT+04, DeviceID);
        outportb(SMPORT+03, oREG_INDEX);
        outportb(SMPORT+05, oREG_DATA);
        outportb(SMPORT+02, 0x48);

        iError = 0;
        do
        {
                iError++;
                if( iError > 0x8000)       return;
                if( ( inportb(SMPORT+0x00) & 0x06 ) == 0x06 )        return;
        }
        while( (inportb(SMPORT+0x00) & 0x06 ) != 0x02 );

}
```

Appendix E: Digital I/O Setting

Below are the source codes written in C, please take them for Digital I/O application examples. The default I/O address is 6Eh.

```
/*-----  Include Header Area -----*/
#include "math.h"
#include "stdio.h"
#include "dos.h"

#define   DELAY_TIME                          10

int SMB_PORT_AD    = 0xF040;
int SMB_DEVICE_ADD = 0x6e; /* 75111R's Add=6eh */

unsigned char DIO_Set(unsigned char oMode, unsigned char oData);
unsigned char SMB_Byte_READ(int SMPORT, int DeviceID, int iREG_INDEX);
void SMB_Byte_WRITE(int SMPORT, int DeviceID, int oREG_INDEX, int oREG_DATA);

/*-----  routing, sub-routing -----*/
void main()
{
         DIO_Set(0xFF,0xFF);
         delay(2000);

         DIO_Set(0xFF,0x00);
         delay(2000);

         DIO_Set(0xFF,0x55);
         delay(2000);

         DIO_Set(0xFF,0xAA);
         delay(2000);

}

unsigned char DIO_Set(unsigned char oMode, unsigned char oData)
{
         unsigned char bData;

    /* GPIO20~27 pin control */
         SMB_Byte_WRITE(SMB_PORT_AD,SMB_DEVICE_ADD,0x20,oMode);
    delay(DELAY_TIME);

    /* GPIO20~27 pin Data */
         SMB_Byte_WRITE(SMB_PORT_AD,SMB_DEVICE_ADD,0x21,oData);
    delay(DELAY_TIME);

         /* GPIO20~27 pin Status */
         bData = SMB_Byte_READ(SMB_PORT_AD,SMB_DEVICE_ADD,0x22);

    return bData;
}

unsigned char SMB_Byte_READ(int SMPORT, int DeviceID, int iREG_INDEX)
{
         unsigned char iData;
```

```
        unsigned char iFlag;
        int iError = 0;

        do
        {
                outportb(SMPORT+00, 0x1E);
                iFlag = inportb(SMPORT+00);
                if( iError++ > 0x8000 )    return 2;
        }
        while( ( iFlag & 0x9F ) != 0 );

        outportb(SMPORT+04, DeviceID+1);
        outportb(SMPORT+03, iREG_INDEX);
        outportb(SMPORT+02, 0x48);

        iError = 0;
        do
        {
                if( iError++ > 0x8000)     return 2;
                if( ( inportb(SMPORT+0x00) & 0x06 ) == 0x06 )        return 1;
        }
        while( (inportb(SMPORT+0x00) & 0x06 ) != 0x02 );

        iData = inportb(SMPORT+05);

        return iData;
}

void SMB_Byte_WRITE(int SMPORT, int DeviceID, int oREG_INDEX, int oREG_DATA)
{
        unsigned char iFlag;
        int iError = 0;

        do
        {
                outportb(SMPORT+00, 0x1E);
                iFlag = inportb(SMPORT+00);
                if( iError++ > 0x8000 )    return;
        }
        while( ( iFlag & 0x9F ) != 0 );

        outportb(SMPORT+04, DeviceID);
        outportb(SMPORT+03, oREG_INDEX);
        outportb(SMPORT+05, oREG_DATA);
        outportb(SMPORT+02, 0x48);

        iError = 0;
        do
        {
                iError++;
                if( iError > 0x8000)       return;
                if( ( inportb(SMPORT+0x00) & 0x06 ) == 0x06 )        return;
        }
        while( (inportb(SMPORT+0x00) & 0x06 ) != 0x02 );

}
```