
EmSMK-i2403

SMARC 2.0 CPU Module

User's Manual

Version 1.0

2022.08



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Revision History

| Version | Release Time | Description |
|---------|--------------|-----------------|
| 1.0 | 2022.08 | Initial release |

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Copyright Notice

All Rights Reserved.

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Under no circumstances will the manufacturer be liable for any direct, indirect, special, incidental, or consequential damages arising from the use or inability to use the product or documentation, even if advised of the possibility of such damages.

This document contains proprietary information protected by copyright. All rights are reserved. No part of this manual may be reproduced by any mechanical, electronic, or other means in any form without prior written permission of the manufacturer.

Declaration of Conformity CE

The device is compliant to CE regulation of the European Union (EU) directives. A Certificate of Compliance is available by contacting Technical Support.

This product has passed the CE test for environmental specifications when shielded cables are used for external wiring. We recommend the use of shielded cables. This kind of cable is available from ARBOR. Please contact your local supplier for ordering information.

This product has passed the CE test for environmental specifications. Test conditions for passing included the equipment being operated within an industrial enclosure. In order to protect the product from being damaged by ESD (Electrostatic Discharge) and EMI leakage, we strongly recommend the use of CE-compliant industrial enclosure products.

Warning

This is a class B product. In a domestic environment this product may cause radio interference in which case the user may be required to take adequate measures.

FCC Class B

This device complies with Part 15 of the FCC Rules. Operation is subject to the following two conditions:

- (1) This device may not cause harmful interference, and
- (2) This device must accept any interference received, including interference that may cause undesired operation.

NOTE:

This equipment has been tested and found to comply with the limits for a Class B digital device, pursuant to Part 15 of the FCC Rules. These limits are designed to provide reasonable protection against harmful interference when the equipment is operated in a commercial environment. This equipment generates, uses, and can radiate radio frequency energy and, if not installed and used in accordance with the instruction manual, may cause harmful interference to radio communications. Operation of this equipment in a residential area is likely to cause harmful interference in which case the user will be required to correct the interference at his own expense.

RoHS

ARBOR Technology Corp. certifies that all components in its products are in compliance and conform to the European Union's Restriction of Use of Hazardous Substances in Electrical and Electronic Equipment (RoHS) Directive 2002/95/EC.

The above mentioned directive was published on 2/13/2003. The main purpose of the directive is to prohibit the use of lead, mercury, cadmium, hexavalent chromium, polybrominated biphenyls (PBB), and polybrominated diphenyl ethers (PBDE) in electrical and electronic products. Member states of the EU are to enforce by 7/1/2006.

ARBOR Technology Corp. hereby states that the listed products do not contain unintentional additions of lead, mercury, hex chrome, PBB or PBDB that exceed a maximum concentration value of 0.1% by weight or for cadmium exceed 0.01% by weight, per homogenous material. Homogenous material is defined as a substance or mixture of substances with uniform composition (such as solders, resins, plating, etc.). Lead-free solder is used for all terminations (Sn(96-96.5%), Ag(3.0-3.5%) and Cu(0.5%)).

SVHC / REACH

To minimize the environmental impact and take more responsibility to the earth we live, Arbor hereby confirms all products comply with the restriction of SVHC (Substances of Very High Concern) in (EC) 1907/2006 (REACH --Registration, Evaluation, Authorization, and Restriction of Chemicals) regulated by the European Union.

All substances listed in SVHC < 0.1 % by weight (1000 ppm)

Warning

Single Board Computers and their components contain very delicate Integrated Circuits (IC). To protect the Single Board Computer and its components against damage from static electricity, you should always follow the following precautions when handling it:

1. Disconnect your Single Board Computer from the power source when you want to work on the inside.
2. Hold the board by the edges and try not to touch the IC chips, leads or circuitry.
3. Use a grounded wrist strap when handling computer components.
4. Place components on a grounded antistatic pad or on the bag that comes with the Single Board Computer, whenever components are separated from the system.

Replacing the Lithium Battery

Incorrect replacement of the lithium battery may lead to a risk of explosion.

The lithium battery must be replaced with an identical battery or a battery type recommended by the manufacturer.

Do not throw lithium batteries into the trash-can. It must be disposed of in accordance with local regulations concerning special waste.

Technical Support

If you have any technical difficulties, please do not hesitate to call or e-mail our customer service.

<http://www.arbor-technology.com>

E-mail: info@arbor.com.tw

Warranty

This product is warranted to be in good working order for a period of two years from the date of purchase. Should this product fail to be in good working order at any time during this period, we will, at our option, replace or repair it at no additional charge except as set forth in the following terms. This warranty does not apply to products damaged by misuse, modifications, accident or disaster.

Vendor assumes no liability for any damages, lost profits, lost savings or any other incidental or consequential damage resulting from the use, misuse of, or inability to use this product. Vendor will not be liable for any claim made by any other related party. Vendors disclaim all other warranties, either expressed or implied, including but not limited to implied warranties of merchantability and fitness for a

particular purpose, with respect to the hardware, the accompanying product's manual(s) and written materials, and any accompanying hardware. This limited warranty gives you specific legal rights.

Return authorization must be obtained from the vendor before returned merchandise will be accepted. Authorization can be obtained by calling or faxing the vendor and requesting a Return Merchandise Authorization (RMA) number. Returned goods should always be accompanied by a clear problem description.

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Chapter 1

Introduction

1.1. The Product

- Onboard Intel Atom x7-E3950/ x5-E3940/ x5-E3930 processor
- Support 4 x PCIe1 lanes
- Support one Ethernet
- Support 1 x eDP, 1 x HDMI, 1 x DP++
- Extended Range Operating Temperature: -20 ~85°C

1.2. About this Manual

This manual is intended for experienced users and integrators with hardware knowledge of computers. If you are not sure about the description in this manual, consult your vendor before further handling.

We recommend that you keep one copy of this manual for the quick reference for any necessary maintenance in the future. Thank you for choosing ARBOR products.

1.3. Specifications

| | |
|--------------------|---|
| Form Factor | SMARC 2.0 CPU Module |
| CPU | Soldered onboard Intel® Atom™ x7-E3950 1.6GHz Atom™ x5-E3940 1.6GHz Atom™ x5-E3930 1.3GHz Processor |
| Memory | Soldered onboard 8GB LPDDR4 SDRAM |
| BIOS | AMI BIOS |
| Watchdog Timer | 1~255 levels reset |
| USB | 6 x USB 2.0 ports 2 x USB 3.0 ports |
| Expansion | 4 x PCIe1 lanes, SDIO, I ² S, I ² C, SMBus |
| GPIO | 8-bit Programmable |
| Serial Port | 4 x UART ports (2 x HSUART, 2 x UART) |
| Storage | 1 x Serial ATA port Soldered onboard eMMC (OEM request) |
| Ethernet | 1 x Intel i210IT PCIe controller |
| Audio | HD Audio Link |
| Graphics Chipset | SoC integrated Intel Gen9 graphic |
| Graphics Interface | 1 x eDP, 1 x DP++, 1 x HDMI port |
| MIPI-CSI | 1 x MIPI-CSIx4 & 1 x MIPI-CSIx2 (OEM request) |
| OS Support | Windows 10 Linux |
| Power Requirement | +3~5.25V power input |
| Power Consumption | 0.71A@5.25V (X7-E3950 typical CPU module only) |
| Operating Temp. | -20 ~ 85°C (-4 ~ 185°F) |
| Operating Humidity | 10 ~ 95% @ 85°C (non-condensing) |
| Dimension (L x W) | 82 x 50 mm |

1.4. Inside the Package

Before starting with the installation, make sure the following items are shipped. If any of the items is missing or appears damaged, contact your local dealer or distributor.



1 x EmSMK-i2403 CPU Module



1 x Quick Installation Guide

1.5. Ordering Information

| | |
|-----------------------|---|
| EmSMK-i2403-E3950-8GB | Intel® Atom™ Processor x7-E3950 SMARC R2.0 CPU module w/ 8GB memory down, -20 ~85°C |
| EmSMK-i2403-E3940-8GB | Intel® Atom™ Processor x5-E3940 SMARC R2.0 CPU module w/ 8GB memory down, -20 ~85°C |
| EmSMK-i2403-E3930-8GB | Intel® Atom™ Processor x5-E3930 SMARC R2.0 CPU module w/ 8GB memory down, -20 ~85°C |

1.6. Optional Accessories

| | |
|----------------|---|
| PBS-9015 | SMARC R2.0 Carrier Board |
| HS-2403-F1 | Heat spreader |
| CBK-02-9015-00 | Cable kit: 1 x COM Cable 1 x SATA Cable |

1.7. Driver Installation Note

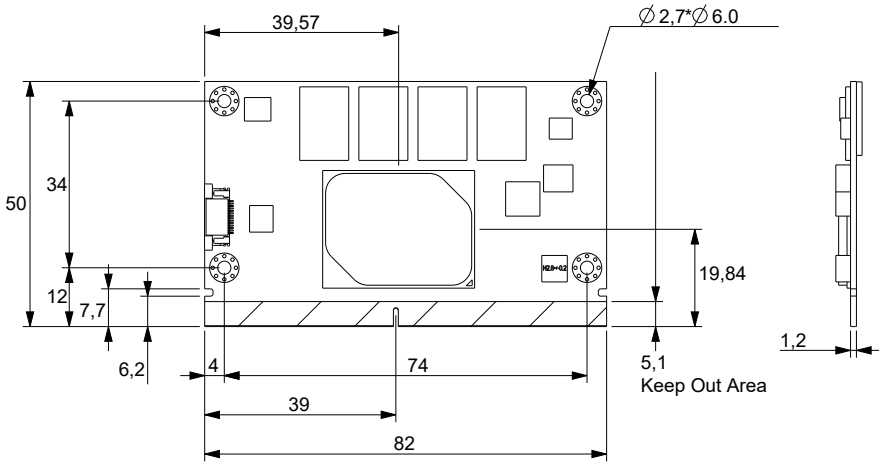
The CPU module supports Windows 10. To install the drivers, please visit our website at **www.arbor-technology.com** and download the driver pack from the **Download Center**. If you need login access, please contact your local ARBOR sales representative.

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Chapter 2

Board Overview

2.1. Board Dimensions

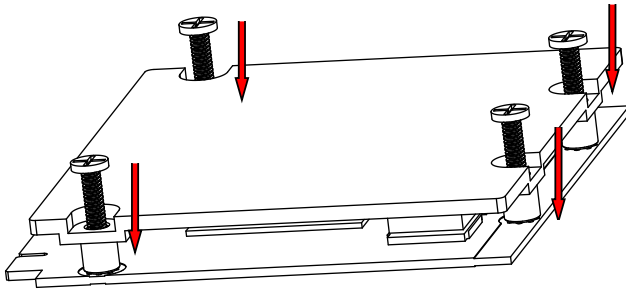


Unit: mm

2.2. Heat Spreader Installation

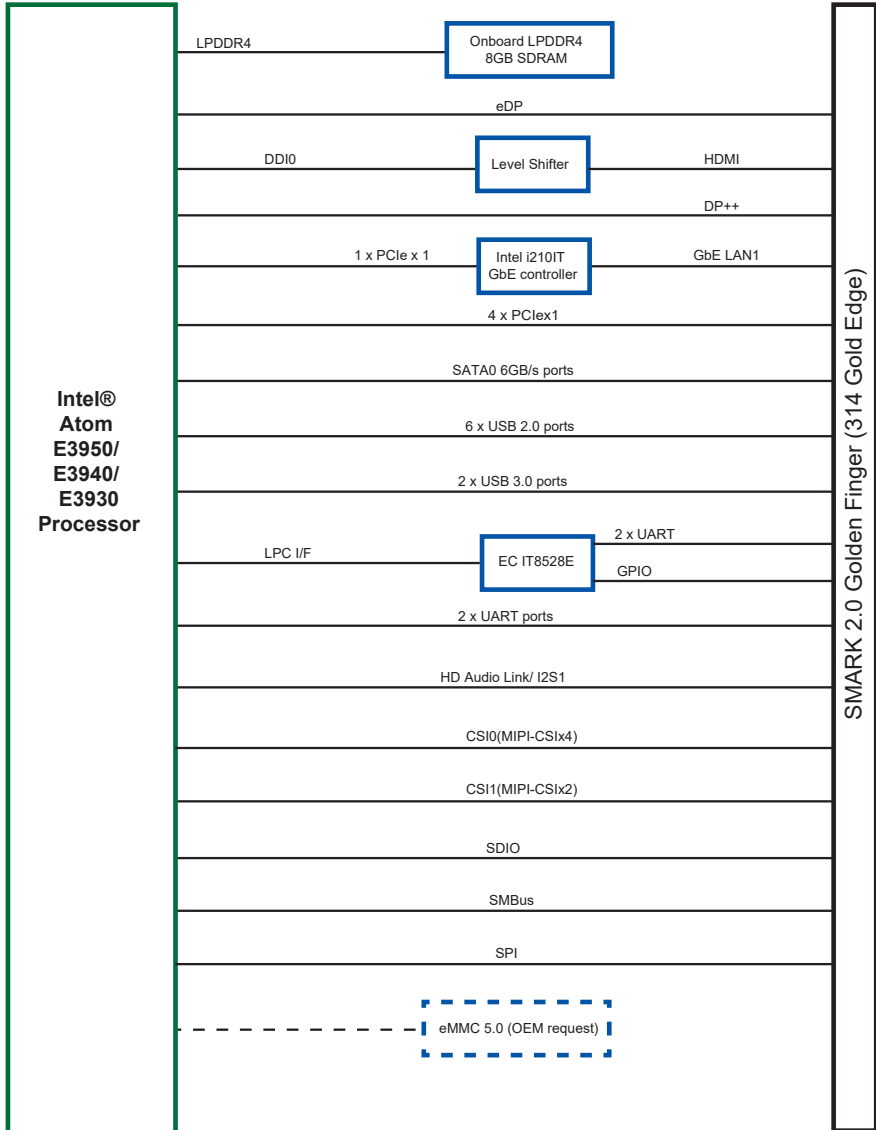
To install the heat spreader:

See the illustration below. Mount the heat spreader to the board. Fix the heat spreader in place with four screws.



2.3. Block Diagram

EmSMK-i2403
SMARC R2.0 CPU module



2.4. Connector Pin Assignment

| P-Pin | Primary (Top) Side | S-Pin | Secondary (Bottom) Side | P-Pin | Primary (Top) Side | S-Pin | Secondary (Bottom) Side |
|-------|--------------------|-------|-------------------------|-------|--------------------|-------|-------------------------|
| P1 | SMB_ALERT_1V8# | S1 | CAM1_SCL | P31 | NC | S31 | NC |
| P2 | GND1 | S2 | CAM1_SDA | P32 | GND6 | S32 | PCIE_D_RX+ |
| P3 | CSI1_CK+ | S3 | GND25 | P33 | SDIO_WP | S33 | PCIE_D_RX- |
| P4 | CSI1_CK- | S4 | RSVD5 | P34 | SDIO_CMD | S34 | GND30 |
| P5 | NC | S5 | CAM0_SCL | P35 | SDIO_CD# | S35 | USB4+ |
| P6 | GBE0_SDP | S6 | CAM_MCK | P36 | SDIO_CK | S36 | USB4- |
| P7 | CSI1_RX0+ | S7 | CAM0_SDA | P37 | SDIO_PWR_EN | S37 | USB3_VBUS_DET |
| P8 | CSI1_RX0- | S8 | CSI0_CK+ | P38 | GND7 | S38 | AUDIO_MCK |
| P9 | GND2 | S9 | CSI0_CK- | P39 | SDIO_D0 | S39 | I2S0_LRCK |
| P10 | CSI1_RX1+ | S10 | GND26 | P40 | SDIO_D1 | S40 | I2S0_SDOUT |
| P11 | CSI1_RX1- | S11 | CSI0_RX0+ | P41 | SDIO_D2 | S41 | I2S0_SDIN |
| P12 | GND3 | S12 | CSI0_RX0- | P42 | SDIO_D3 | S42 | I2S0_CK |
| P13 | CSI1_RX2+ | S13 | GND27 | P43 | SPI0_CS0# | S43 | ESPI_ALERT0# |
| P14 | CSI1_RX2- | S14 | CSI0_RX1+ | P44 | SPI0_CK | S44 | ESPI_ALERT1# |
| P15 | GND4 | S15 | CSI0_RX1- | P45 | SPI0_DIN | S45 | NC |
| P16 | CSI1_RX3+ | S16 | GND28 | P46 | SPI0_DO | S46 | NC |
| P17 | CSI1_RX3- | S17 | NC | P47 | GND8 | S47 | GND31 |
| P18 | GND5 | S18 | NC | P48 | SATA_TX+ | S48 | I2C_GP_CK |
| P19 | GBE_MDI3- | S19 | NC | P49 | SATA_TX- | S49 | I2C_GP_DAT |
| P20 | GBE_MDI3+ | S20 | NC | P50 | GND9 | S50 | HDA_SYNC |
| P21 | GBE_LINK100# | S21 | NC | P51 | SATA_RX+ | S51 | HDA_SDO |
| P22 | GBE_LINK1000# | S22 | NC | P52 | SATA_RX- | S52 | HDA_SDI |
| P23 | GBE_MDI2- | S23 | NC | P53 | GND10 | S53 | HDA_CLK |
| P24 | GBE_MDI2+ | S24 | NC | P54 | ESPI_CS0# | S54 | SATA_ACT# |
| P25 | GBE_LINK_ACT# | S25 | GND29 | P55 | ESPI_CS1# | S55 | USB5_EN_OC# |
| P26 | GBE_MDI1- | S26 | NC | P56 | ESPI_CK | S56 | NC |
| P27 | GBE_MDI1+ | S27 | NC | P57 | ESPI_IO_0 | S57 | NC |
| P28 | NC | S28 | NC | P58 | ESPI_IO_1 | S58 | ESPI_RESET# |
| P29 | GBE_MDI0- | S29 | PCIE_D_TX+ | P59 | GND11 | S59 | USB5+ |
| P30 | GBE_MDI0+ | S30 | PCIE_D_TX- | P60 | USB0+ | S60 | USB5- |
| | | | | P61 | USB0- | S61 | GND32 |
| | | | | P62 | USB0_EN_OC# | S62 | USB3_SSTX+ |
| | | | | P63 | USB_VBUS_DET | S63 | USB3_SSTX- |

Board Overview

| P-Pin | Primary (Top) Side | S-Pin | Secondary (Bottom) Side | P-Pin | Primary (Top) Side | S-Pin | Secondary (Bottom) Side |
|-------|--------------------|-------|-------------------------|-------|--------------------|-------|-------------------------|
| P64 | USB0_OTG_ID | S64 | GND33 | P94 | GND18 | S94 | DP0_LANE0- |
| P65 | USB1+ | S65 | USB3_SSRX+ | P95 | SMARC_HDMI1_TXP1 | S95 | DP0_AUX_SEL |
| P66 | USB1- | S66 | USB3_SSRX- | P96 | SMARC_HDMI1_TXN1 | S96 | DP0_LANE1+ |
| P67 | USB1_EN_OC# | S67 | GND34 | P97 | GND19 | S97 | DP0_LANE1- |
| P68 | GND12 | S68 | USB3+ | P98 | SMARC_HDMI1_TXP0 | S98 | DP0_HPD |
| P69 | USB2+ | S69 | USB3- | P99 | SMARC_HDMI1_TXN0 | S99 | DP0_LANE2+ |
| P70 | USB2- | S70 | GND35 | P100 | GND20 | S100 | DP0_LANE2- |
| P71 | USB2_EN_OC# | S71 | USB2_SSTX+ | P101 | SMARC_HDMI1_TXP3 | S101 | GND42 |
| P72 | RSVD1 | S72 | USB2_SSTX- | P102 | SMARC_HDMI1_TXN3 | S102 | DP0_LANE3+ |
| P73 | NC | S73 | GND36 | P103 | GND21 | S103 | DP0_LANE3- |
| P74 | NC | S74 | USB2_SSRX+ | P104 | SMARC_DDI1_HPDET | S104 | USB3_OTG_ID |
| P75 | PCIE_A_RST# | S75 | USB2_SSRX- | P105 | SMARC_DDI1_AUXP | S105 | DP0_AUX+ |
| P76 | USB4_EN_OC# | S76 | PCIE_B_RST# | P106 | SMARC_DDI1_AUXN | S106 | DP0_AUX- |
| P77 | NC | S77 | PCIE_C_RST# | P107 | DDI1_DDC_AUX_SEL | S107 | NC |
| P78 | NC | S78 | PCIE_C_RX+ | P108 | GPIO0 | S108 | NC |
| P79 | GND13 | S79 | PCIE_C_RX- | P109 | GPIO1 | S109 | NC |
| P80 | PCIE_C_REFCK+ | S80 | GND37 | P110 | GPIO2 | S110 | GND43 |
| P81 | PCIE_C_REFCK- | S81 | PCIE_C_TX+ | P111 | GPIO3 | S111 | NC |
| P82 | GND14 | S82 | PCIE_C_TX- | P112 | HDA_RST# | S112 | NC |
| P83 | PCIE_A_REFCK+ | S83 | GND38 | P113 | FAN_PWMOUT | S113 | NC |
| P84 | PCIE_A_REFCK- | S84 | PCIE_B_REFCK+ | P114 | FAN_TACHIN | S114 | NC |
| P85 | GND15 | S85 | PCIE_B_REFCK- | P115 | GPIO7 | S115 | NC |
| P86 | PCIE_A_RX+ | S86 | GND39 | P116 | GPIO8 | S116 | NC |
| P87 | PCIE_A_RX- | S87 | PCIE_B_RX+ | P117 | GPIO9 | S117 | NC |
| P88 | GND16 | S88 | PCIE_B_RX- | P118 | GPIO10 | S118 | NC |
| P89 | PCIE_A_TX+ | S89 | GND40 | P119 | GPIO11 | S119 | GND44 |
| P90 | PCIE_A_TX- | S90 | PCIE_B_TX+ | P120 | GND22 | S120 | NC |
| P91 | GND17 | S91 | PCIE_B_TX- | P121 | I2C_PM_CK | S121 | NC |
| P92 | SMARC_HDMI1_TXP2 | S92 | GND41 | P122 | I2C_PM_DAT | S122 | NC |
| P93 | SMARC_HDMI1_TXN2 | S93 | DP0_LANE0+ | P123 | BOOT_SEL0# | S123 | NC |
| | | | | P124 | BOOT_SEL1# | S124 | GND44 |

| P-Pin | Primary (Top) Side | S-Pin | Secondary (Bottom) Side |
|--------------|-------------------------------|--------------|------------------------------------|
| P125 | BOOT_SEL2# | S125 | eDP_TX0_P |
| P126 | RESET_OUT# | S126 | eDP_TX0_N |
| P127 | RESET_IN# | S127 | LCD_BKLT_EN |
| P128 | POWER_BTN# | S128 | eDP_TX1_P |
| P129 | SER0_TX | S129 | eDP_TX1_N |
| P130 | SER0_RX | S130 | GND46 |
| P131 | SER0_RTS# | S131 | eDP_TX2_P |
| P132 | SER0_CTS# | S132 | eDP_TX2_N |
| P133 | GND23 | S133 | LCD_VDD_EN |
| P134 | SER1_TX | S134 | eDP_AUX_P |
| P135 | SER1_RX | S135 | eDP_AUX_N |
| P136 | SER2_TX | S136 | GND47 |
| P137 | SER2_RX | S137 | eDP_TX3_P |
| P138 | SER2_RTS# | S138 | eDP_TX3_N |
| P139 | SER2_CTS# | S139 | NC |
| P140 | SER3_TX | S140 | NC |
| P141 | SER3_RX | S141 | LCD_BKLT_PWM |
| P142 | GND24 | S142 | NC |
| P143 | NC | S143 | GND48 |
| P144 | NC | S144 | eDP0_HPD |
| P145 | NC | S145 | WDT_TIME_OUT# |
| P146 | NC | S146 | PCIE_WAKE# |
| P147 | VDD_IN1 | S147 | VDD_RTC |
| P148 | VDD_IN2 | S148 | LID# |
| P149 | VDD_IN3 | S149 | SLEEP# |
| P150 | VDD_IN4 | S150 | VIN_PWR_BAD# |
| P151 | VDD_IN5 | S151 | CHARGING# |
| P152 | VDD_IN6 | S152 | CHARGER_ PRSNT# |
| P153 | VDD_IN7 | S153 | CARRIER_STBY# |
| P154 | VDD_IN8 | S154 | CARRIER_PWR_ON |
| P155 | VDD_IN9 | S155 | FORCE_RECOV# |
| P156 | VDD_IN10 | S156 | BATLOW# |
| | | S157 | TEST# |
| | | S158 | GND49 |

Chapter 3

BIOS

The BIOS Setup utility is featured by AMI BIOS to configure the system settings stored in the system's BIOS ROM. AMI BIOS is activated once the computer powers on.

After entering the utility, use the left/right arrow keys to navigate between the top menus and use the down arrow key to access one.

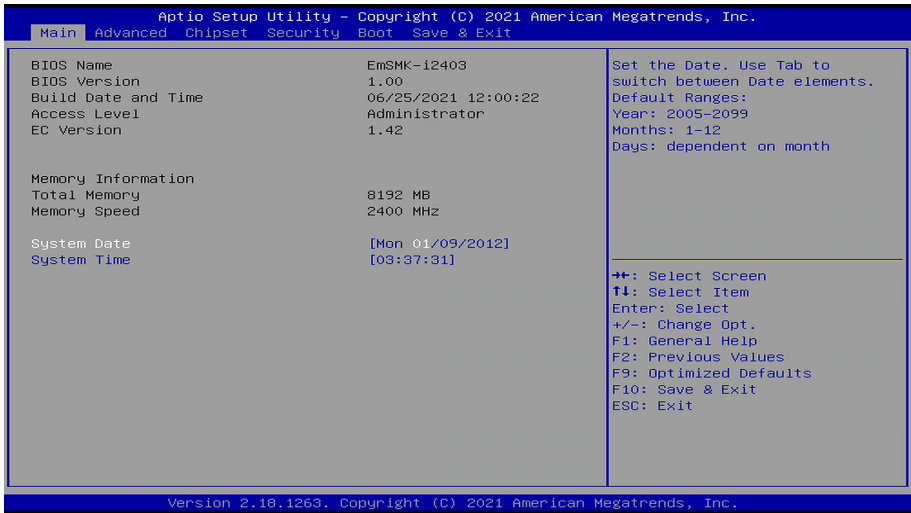
| Menu | Description |
|------------------------|--|
| Main | See 3.1 Main on page 16 . |
| Advanced | See 3.2 Advanced on page 18 . |
| Chipset | See 3.3 Chipset on page 36 . |
| Security | See 3.4 Security on page 48 . |
| Boot | See 3.5 Boot on page 49 . |
| Save & Exit | See 3.6 Save & Exit on page 50 . |

NOTE: For system stability and performance, this BIOS utility is constantly improved. The screenshots demonstrated and descriptions hereinafter are for reference only and may not exactly meet what is presented onscreen.

3.1 Main

The AMI BIOS provides a Setup utility program for specifying the system configurations and settings. The BIOS RAM of the system stores the Setup utility and configurations. When you turn on the computer, the AMI BIOS is immediately activated. To enter the BIOS SETUP UTILITY, press **“Delete”** once the power is turned on. When the computer is shut down, the battery on the motherboard supplies the power for BIOS RAM.

The **Main Setup** screen lists the following information:



| Info Item | Description |
|----------------------------|---|
| BIOS Name | Delivers the Project name. |
| BIOS Version | Delivers the version of BIOS. |
| Build Date and Time | Delivers the date and time the BIOS Setup utility was made/updated. |
| Access Level | Delivers the level by which the BIOS Setup utility is being accessed at the moment. |
| System Date | Sets system date. |
| System Time | Sets system time. |

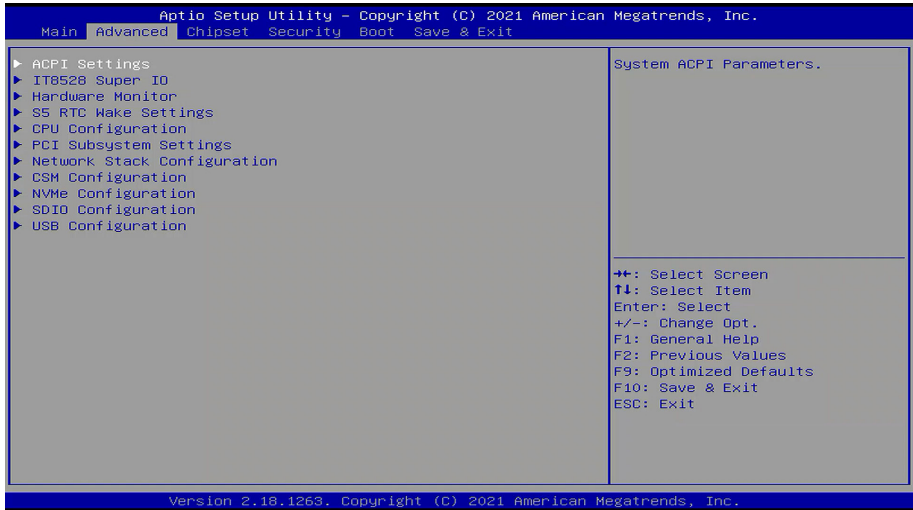
Key Commands

BIOS Setup Utility is mainly a key-based navigation interface. Please refer to the following key command instructions for navigation process.

| Keystroke | Function |
|-------------|---|
| ◀ ▶ | Move to highlight a particular configuration screen from the top menu bar / Move to highlight items on the screen |
| ▼ ▲ | Move to highlight previous/next item |
| Enter | Select and access a setup item/field |
| Esc | On the Main Menu – Quit the setup and not save changes into CMOS (a message screen will display and ask you to select “OK” or “Cancel” for exiting and discarding changes. Use “←” and “→” to select and press “Enter” to confirm) On the Sub Menu – Exit current page and return to main menu |
| Page Up / + | Increase the numeric value on a selected setup item / make change |
| Page Down - | Decrease the numeric value on a selected setup item / make change |
| F1 | Activate “General Help” screen |
| F0 | Save the changes that have been made in the setup and exit. (a message screen will display and ask you to select “OK” or “Cancel” for exiting and saving changes. Use “←” and “→” to select and press “Enter” to confirm) |

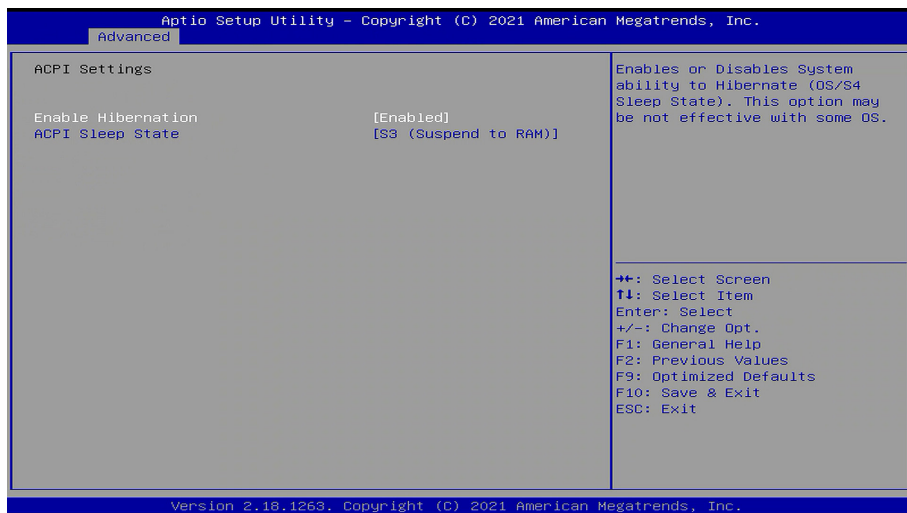
3.2 Advanced

The “Advanced” setting page provides you the options to configure the details of your hardware, such as ACPI, CPU, SATA, AMT, USB and Super IO.



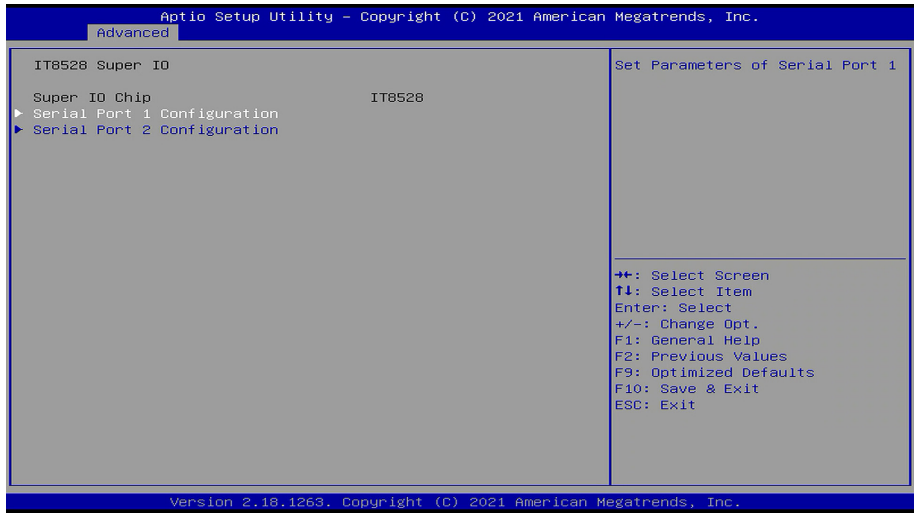
| Setting | Description |
|------------------------------------|--|
| ACPI Settings | See 3.2.1 ACPI Settings on the page 19 |
| IT8528 Super IO | See 3.2.2 IT8528 Super IO on page 20 |
| Hardware Monitor | See 3.2.3 Hardware Monitor on page 22 |
| S5 RTC Wake Settings | See 3.2.4 S5 RTC Wake Settings on page 23 |
| CPU Configuration | See 3.2.5 CPU Configuration on page 24 |
| PCI Subsystem Settings | See 3.2.6 PCI Subsystem Settings on page 25 |
| Network Stack Configuration | See 3.2.7 Network Stack Configuration on page 30 |
| CSM Configuration | See 3.2.8 CSM Configuration on page 31 |
| NVMe Configuration | See 3.2.9 NVMe Configuration on page 32 |
| SDIO Configuration | See 3.2.10 SDIO Configuration on page 33 |
| USB Configuration | See 3.2.11 USB Configuration on page 34 |

3.2.1 ACPI Settings



| Setting | Description |
|--------------------|---|
| Enable Hibernation | Enables (default) or Disables System ability to Hibernate (OS/S4 Sleep State). This option may be not effective with some OS. |
| ACPI Sleep State | Select ACPI sleep state the system will enter when the SUSPEND button is pressed. <ul style="list-style-type: none"> Options: Suspend Disabled and S3 (Suspend to RAM) (default). |

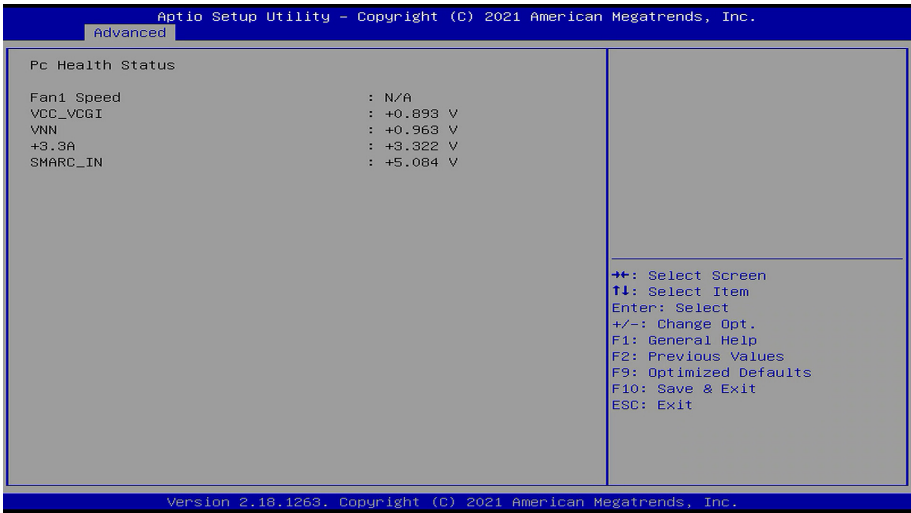
3.2.2 IT8528 Super IO



| Setting | Description | |
|-----------------------------|-------------------------------------|--|
| Serial Port 1 Configuration | Set the Parameters of Serial Port 1 | |
| | Serial Port | Enable or disable Serial Port. ▶ Enabled is the default. |
| | Change Setting | Select an optimal setting for Super IO device. ▶ Options for Serial Port 1: Auto; IO=3F8h; IRQ=4 (default); IO=3F8h; IRQ=3, 4, 10, 11, 12; IO=2F8h; IRQ=3, 4, 10, 11, 12; IO=3E8h; IRQ=3, 4, 10, 11, 12; IO=2E8h; IRQ=3, 4, 10, 11, 12; |

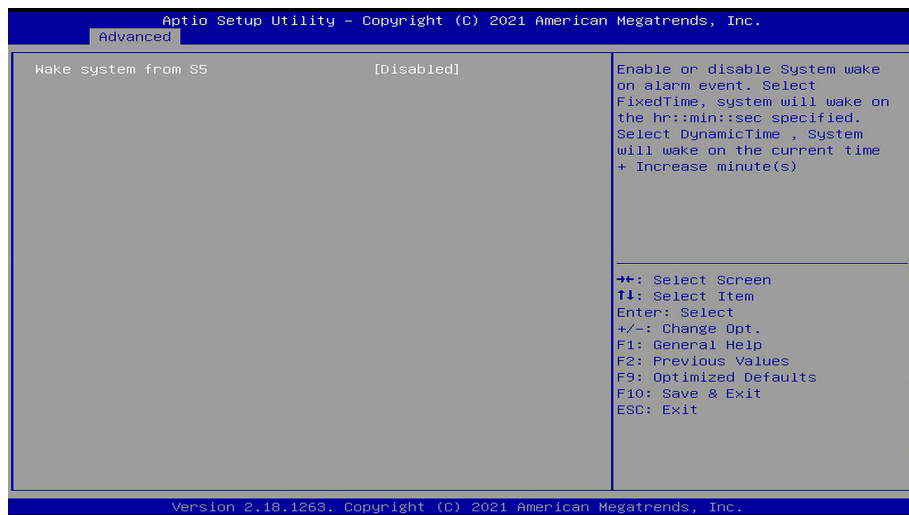
| | | |
|--------------------------------|-------------------------------------|---|
| Serial Port 2 Configuration | Set the Parameters of Serial Port 2 | |
| | Serial Port | Enable or disable Serial Port. ▶ Enabled is the default. |
| | Change Setting | Select an optimal setting for Super IO device. ▶ Options for Serial Port 1: Auto; IO=2F8h; IRQ=3 (default) ; IO=3F8h; IRQ=3, 4, 10, 11, 12; IO=2F8h; IRQ=3, 4, 10, 11, 12; IO=3E8h; IRQ=3, 4, 10, 11, 12; IO=2E8h; IRQ=3, 4, 10, 11, 12; |

3.2.3 Hardware Monitor



Select this submenu to view the main board's hardware status.

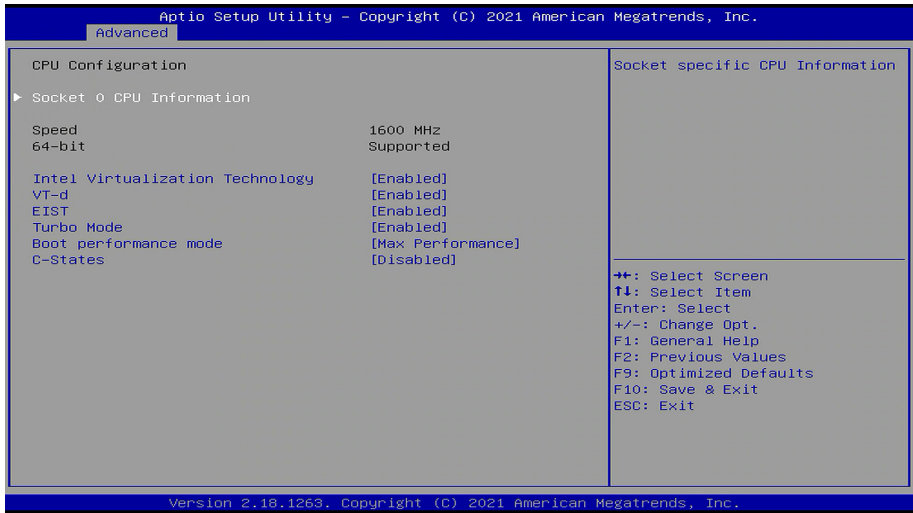
3.2.4 S5 RTC Wake Settings



| Setting | Description |
|---------------------|---|
| Wake System from S5 | <p>Enable or Disable (default) system wake on alarm event.</p> <ul style="list-style-type: none"> Options available are: <p>Disabled (default):</p> <p>Fixed Time: System will wake on the hr::min::sec specifiedc.</p> <p>DynamicTime: If selected, you need to set Wake up minute increase from 1 - 5. System will wake on the current time increase minute(s).</p> |

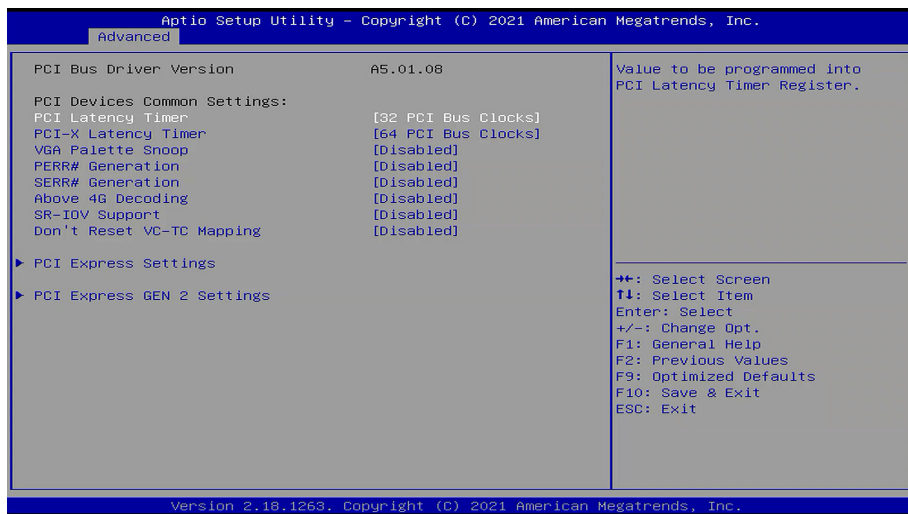
3.2.5 CPU Configuration

Access this submenu to configure the CPU features.



| Setting | Description |
|---------------------------------|---|
| Socket 0 CPU Information | Display Socket specific CPU Information. |
| Intel Virtualization Technology | When enable, a VMM can utilize the additional hardware capabilities provided by Vanderpool Technology ▶ Enabled is the default. |
| VT-D | Enable/Disable CPU VT-D ▶ Enabled is the default. |
| EIST | Enables/Disables Intel SpeedStep ▶ Enabled is the default. |
| Turbo Mode | Enables/Disables Turbo Mode ▶ Enabled is the default. |
| Boot performance mode | Select the performance state that the BIOS will set before OS handoff. ▶ Options: Max performance (default), Max Battery |
| C-States | Enables/disables C states. ▶ Enabled is the default. |

3.2.6 PCI Subsystem Settings

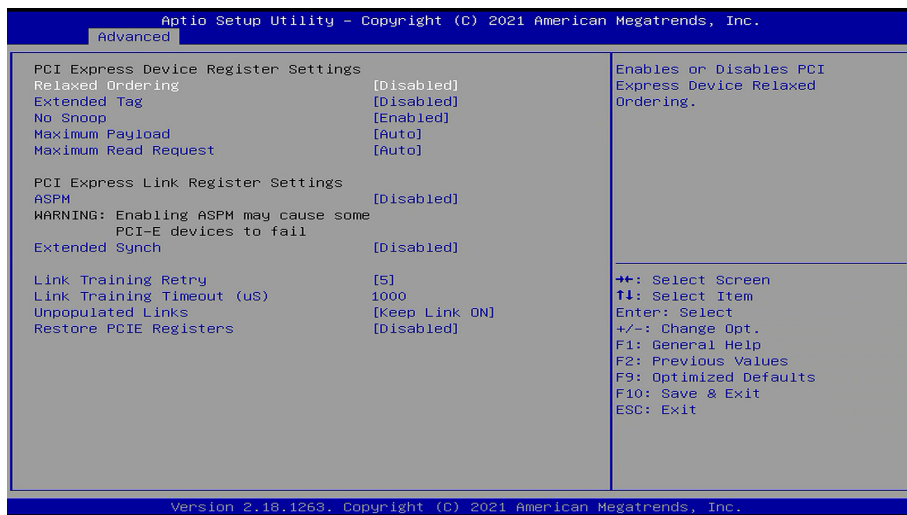


The featured submenus are:

| Setting | Description |
|---------------------|--|
| PCI Latency Timer | Value to be programmed into PCI Latency Timer Register. ► Options: 32 (default), 64, 96, 128, 160, 192, 224 and 248 PCI Bus Clocks. |
| PCI-X Latency Timer | Value to be programmed into PCI-X Latency Timer Register. ► Options: 32, 64(default), 96, 128, 160, 192, 224 and 248 PCI Bus Clocks. |
| VGA Palette Snoop | Enable/Disable (default) VGA Palette Registers Snooping. |
| Perr# Generation | Enable/Disable (default) PCI device to Generate PERR#. |
| Serr# Generation | Enable/Disable (default) PCI device to Generate SERR#. |
| Above 4G Decoding | Enable (default)/ Disable 64bit capable Devices to be Decoded in Above 4G Address Space (Only if System Supports 64 bit PCI Decoding). |

| | |
|---------------------------|---|
| SR-IOV Support | If system has SR-IOV capable PCIe devices, this option Enables or Disables single root IO virtualization support. |
| Don't Reset VC-TC Mapping | If system has Virtual Channels, software can reset traffic class mapping. ▶ Disabled is the default. |
| PCI Express Setting | See next page |
| PCI Express GEN2 Setting | Supports 64 bit (PCI Decoding). |
| | |

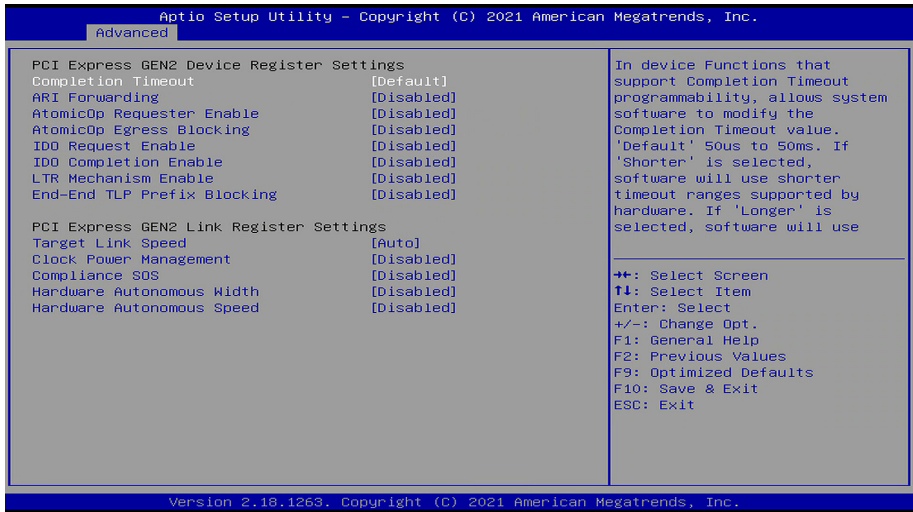
3.2.6.1 PCI Express Settings



The featured submenus are:

| Setting | Description |
|-------------------------|---|
| Relaxed Ordering | Enabled or Disabled (default) Relaxed Ordering. |
| Extended Tag | Enabled or Disabled (default) Extended Tag. |
| No Snoop | Enabled (default)/ Disabled No Snoop. |
| Maximum Payload | This item allows users to set the Maximum Payload. |
| Maximum Payload Request | This item allows users to set the Maximum Read Request Size of PCI Express Device or allow system BIOS to select the value. |
| ASPM Support | Enabled/Disabled (default) or Auto ASPM Support. |
| Extended Synch | Enabled or Disable (default) Extended Synch. |
| Link Training Retry | This item allows users to set the Link Training Retry |
| Training Retry Timeout | This item allows users to set the Link Training Timeout (uS) |
| Unpopulated Links | This item allows users to set the Unpopulated Links |
| Restore PCIE Registers | Enabled or Disabled PCI Express device relaxed ordering. |

3.2.6.2 PCI Express GEN 2 Settings

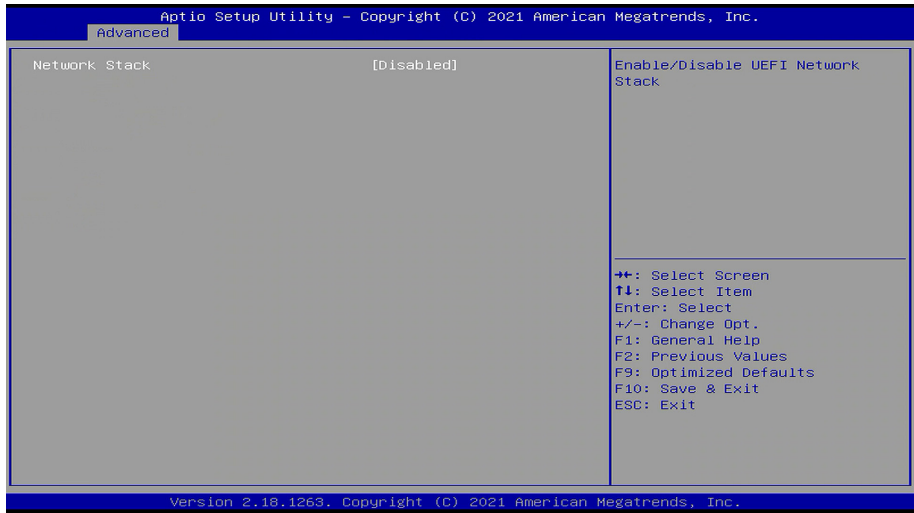


The featured submenus are:

| Setting | Description |
|--|---|
| PCI Express GEN2 Device Register Settings | |
| Completion Time out | In device functions that support Completion Timeout programmability, allows system software to modify the Completion Timeout value. ▶ Default is the default. "Default": 50us to 50ms. |
| ARI Forwarding | If supported by hardware and set to "Enabled", the Downstream Port disables its traditional Device Number field being 0 enforcement when turning a Type1 Configuration Request into a Type0 Configuration Request, permitting access to Extended Functions in an ARI Device immediately below the Port. ▶ Disabled is the default |
| AtomicOp Requester Enable | If supported by hardware and set to "Enabled", this function initiates AtomicOp Requests only if Bus Master Enable bit is in the Command Register Set. ▶ Disabled is the default |
| AtimucOp Egress Blocking | If supported by hardware and set to "Enabled", outbound AtomicOp Requests via Egress Ports will be blocked. ▶ Disabled is the default |

| | |
|--|---|
| IDO Request Enable | If supported by hardware and set to “Enabled”, this permits setting the number of ID-Based Ordering (IDO) bit (Attribute[2]) requests to be initiated. ▶ Disabled is the default setting |
| IDO Completion Enable | If supported by hardware and set to “Enabled”, this permits setting the number of ID-Based Ordering (IDO) bit (Attribute[2]) requests to be initiated. ▶ Disabled is the default setting |
| LTR Mechanism Enable | If supported by hardware and set to “Enabled”, this enables the Latency Tolerance Reporting (LTR) Mechanism. ▶ Disabled is the default setting |
| End-End TLP Prefix Blocking | If supported by hardware and set to “ Enabled ”, this function will block forwarding of TLPs containing End-End TLP Prefixes. ▶ Disabled is the default setting |
| PCI Express GEN2 Link Register Settings | |
| Target Link Speed | If supported by hardware and set to “Force to 2.5 GT/s” for Downstream Ports, this sets an upper limit on Link operational speed by restricting the values advertised by the Upstream component in its training sequences. When “ Auto ” is selected HW initialized data will be used. ▶ Auto is the default setting |
| Clock Power Management | If supported by hardware and set to “ Enabled ”, the device is permitted to use CLKREQ# signal for power management of Link clock in accordance to protocol defined in appropriate form factor specification. ▶ Disabled is the default setting |
| Compliance SOS | If supported by hardware and set to “ Enabled ”, this will force LTSSM to send SKP Ordered Sets between sequences when sending Compliance Pattern or Modified Compliance Pattern. ▶ Disabled is the default setting |
| Hardware Autonomous width | If supported by hardware and set to “ Disabled ”, this will disable the hardware’s ability to change link width except width size reduction for the purpose of correcting unstable link operation. ▶ Disabled is the default setting |
| Hardware Autonomous width | If supported by hardware and set to “ Disabled ”, this will disable the hardware’s ability to change link speed except speed rate reduction for the purpose of correcting unstable link operation. ▶ Disabled is the default setting |

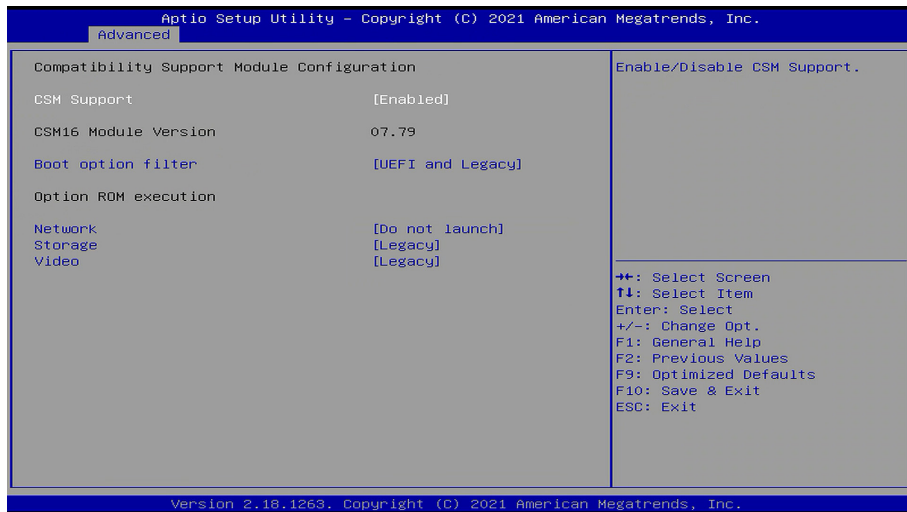
3.2.7 Network Stack Configuration



The featured submenus are:

| Setting | Description |
|---------------|---|
| Network Stack | Enables/disables UEFI network stack. ▶ Disabled is the default setting. |

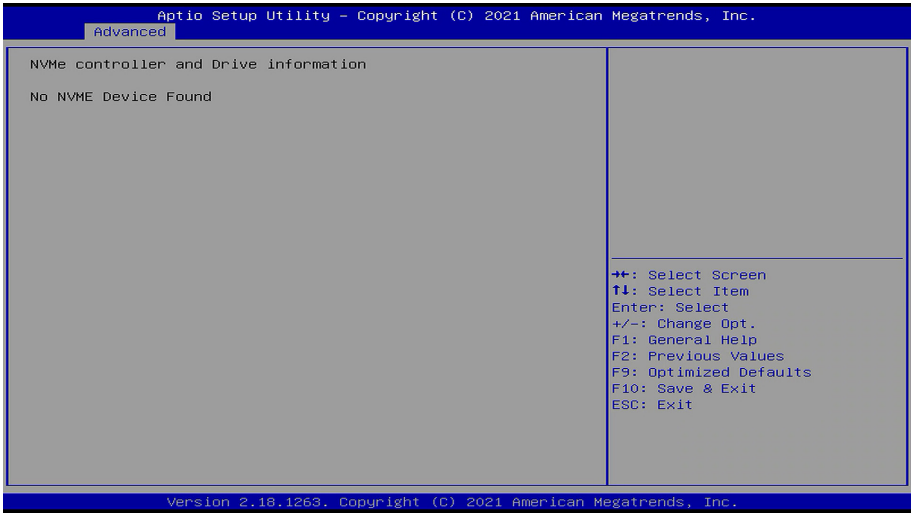
3.2.8 CSM Configuration



The featured submenus are:

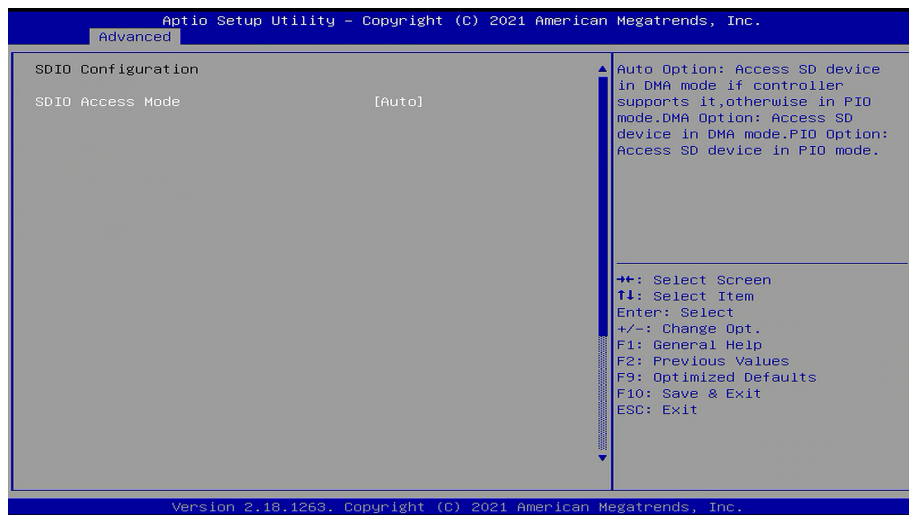
| Setting | Description |
|----------------------|---|
| CSM Support | Enable and Disable CSM Support ► Enabled is the default setting. |
| CSM16 Module Version | Shows the CSM16 module version. |
| Boot option filter | Controls Legacy/UEFI ROMs priority. ► Options: UEFI and Legacy (default), Legacy only and UEFI only |
| Network | Control the execution of UEFI and Legacy PXE OpROM. ► Options: Do not launch (default), UEFI and Legacy . |
| Storage | Control the execution of UEFI and Legacy Storage OpROM. ► Options: Do not launch and Legacy (default). |
| Video | Control the execution of UEFI and Legacy Video OpROM. ► Options: Do not launch , UEFI and Legacy (default). |

3.2.9 NVMe Configuration



Access this submenu to view the NVMe controller and driver information.

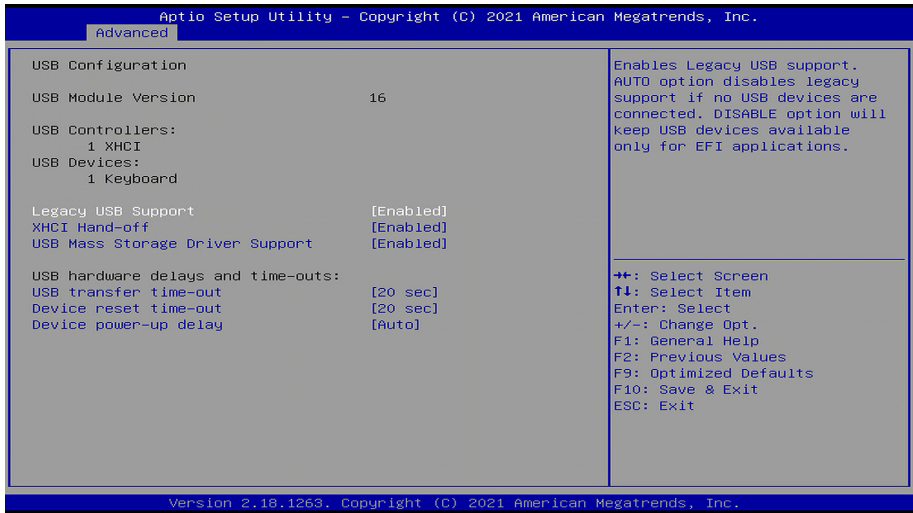
3.2.10 SDIO Configuration



The featured submenus are:

| Setting | Description |
|------------------|---|
| SDIO Access Mode | Configures SDIO Access Mode. Options: <ul style="list-style-type: none"> ▶ Auto: Access SD device in DMA mode if controller supports it, otherwise in PIO mode. ▶ ADMA/SDMA: Access SD device in DMA mode. ▶ PIO: Access SD device in PIO mode. |

3.2.11 USB Configuration



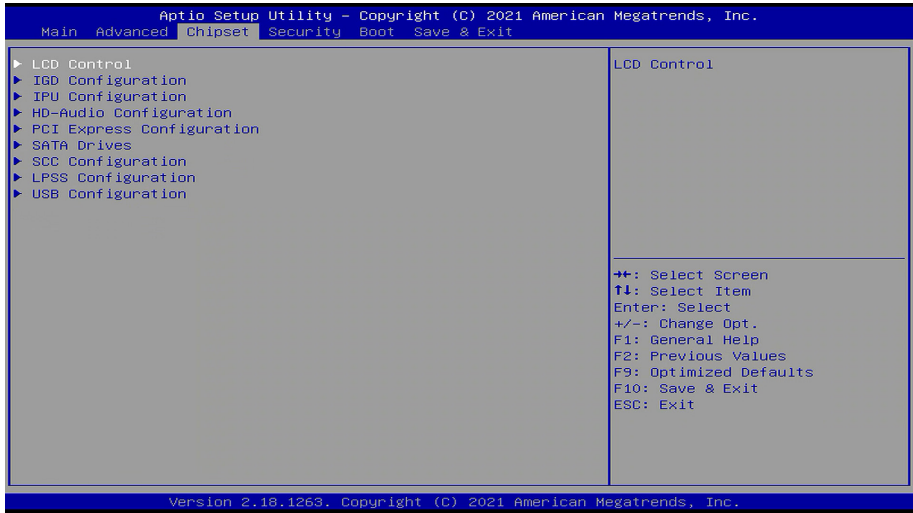
Select this submenu to view the status of the USB ports and configure USB features.

The featured settings and delivered info are:

| Setting / Info | Description |
|---------------------------------|---|
| Legacy USB Support | <p>Enables/disables legacy USB support.</p> <ul style="list-style-type: none"> Options available are Enabled (default), Disabled and Auto. Select Auto to disable legacy support if no USB device are connected. Select Disabled to keep USB devices available only for EFI applications. |
| XHCI Hand-off | <p>Enables/disables a workaround for the operating systems that have no XHCI hand-off support</p> <ul style="list-style-type: none"> Enabled is the default setting. |
| USB Mass Storage Driver Support | <p>Enables/disables the support for USB mass storage driver.</p> <ul style="list-style-type: none"> Enabled is the default setting. |
| USB transfer time-out | <p>The time-out value for Control, Bulk and Interrupt transfers.</p> <ul style="list-style-type: none"> Options: 1/5/10/20 sec (default) |

| | |
|-----------------------|--|
| Device reset time-out | USB mass storage device Start Unit command time-out. ▶ Options: 10/20 (default)/ 30/40 sec |
| Device power-up delay | Maximum time the device will take before it properly reports itself to the Host Controller. 'Auto' uses default value: for a Root port it is 100 ms, for a Hub port the delay is taken from Hub descriptor. ▶ Options: Auto (default), Manual |

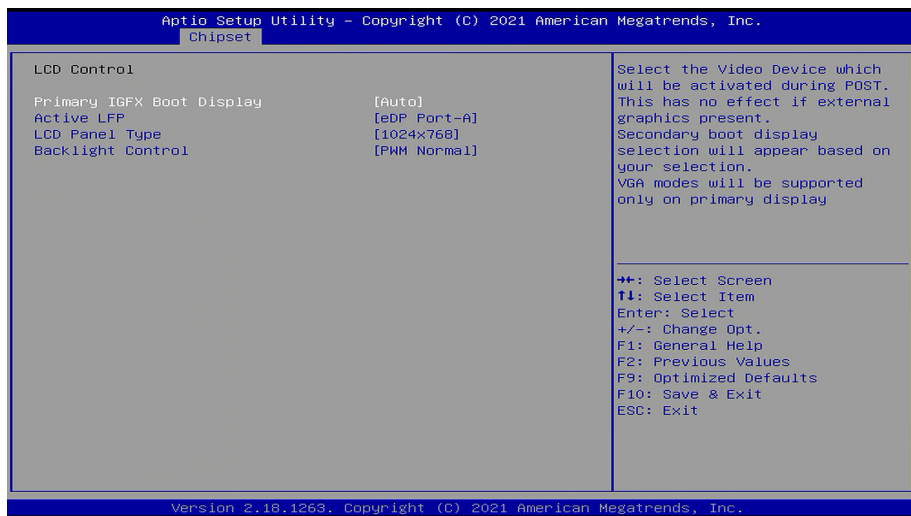
3.3 Chipset



The featured settings and delivered info are:

| Setting | Description |
|---------------------------|--|
| LCD Control | See 3.3.1 LCD Control on page 37 |
| IGD Configuration | See 3.3.2 IGD Configuration on page 39 |
| IPU Configuration | See 3.3.3 IPU Configuration on page 40 |
| HD-Audio Configuration | See 3.3.4 HD-Audio Configuration on page 41 |
| PCI Express Configuration | See 3.3.5 PCI Express Configuration on page 43 |
| SATA Drives | See 3.3.6 SATA Drives on page 44 |
| SCC Configuration | See 3.3.7 SCC Configuration on page 45 |
| LPSS Configuration | See 3.3.8 LPSS Configuration on page 46 |
| USB Configuration | See 3.3.9 USB Configuration on page 47 |

3.3.1 LCD Control

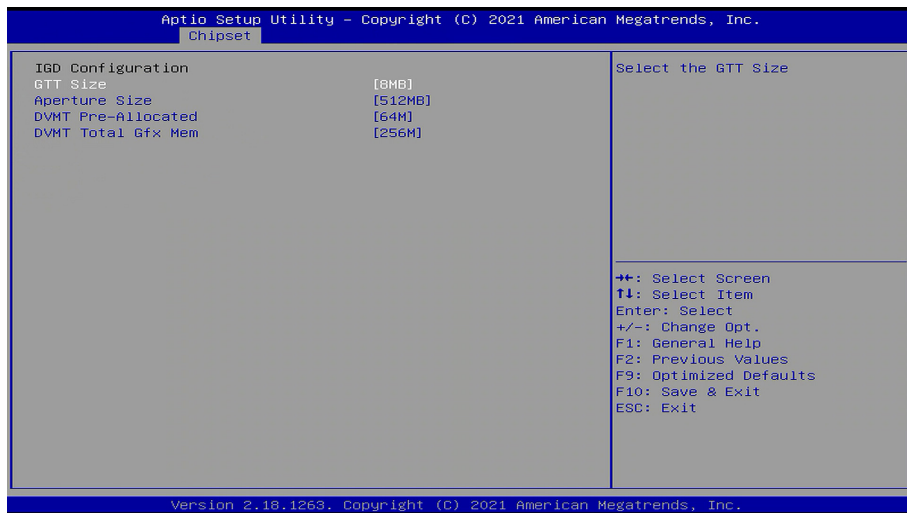


The featured settings and delivered info are:

| Setting | Description |
|---------------------------|--|
| Primary IGFX Boot Display | Select the video device which will be activated during POST. This has no effect if external graphics present. Secondary boot display selection will appear based on your selection. VGA modes will be supported only on primary display. ▶ Options: Auto (default), eDP and LFP . |
| Active LFP | Select the Active LFP Configuration. No LVDS: VBIOS does not enable LVDS. Int-LVDS: VBIOS enables LVDS driver by Integrated encoder. SDVO LVDS: VBIOS enables LVDS driver by SDVO encoder. eDP Port-A: LFP Driven by Int-DisplayPort encoder from Port-A. ▶ Options: No LVDS and eDP Port-A (default) |

| | |
|-------------------|---|
| LCD Panel Type | Select LCD panel used by Internal Graphics Device by selecting the appropriate setup item. Default is 1024x768 . |
| Backlight Control | Select Light Control setting ▶ Options: PWM Normal (default) and PWM Inverted |

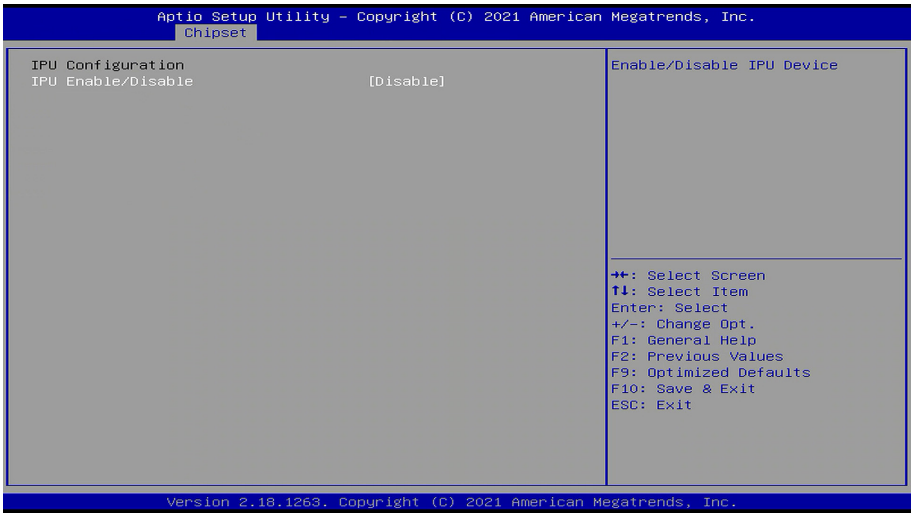
3.3.2 IGD Configuration



The featured settings and delivered info are:

| Item | Description |
|--------------------|--|
| GTT Size | Configures the GTT size ▶ Options: 2M/4M/8M (default) |
| Aperture Size | Configures the aperture size. ▶ Options: 128M/256M/512M (default) |
| DVMT Pre-Allocated | Use the DVMT Pre-Allocated option to set the amount of system memory allocated to the integrated graphics processor when the system boots. The system memory allocated can then only be used as graphics memory, and is no longer available to applications or the operating system. Configuration options are listed below: ▶ Options: 64M (default)/ 96M/128M/160M/192M/224M/256M/288M/320M/352M/384M/416M/448M/480M/512M |
| DVMT Total Gfx Mem | Use the DVMT Total Gfx Mem option to select DVMT5.0 total graphic memory size used by the internal graphic device. The following options are available: ▶ Options: 128MB/256MB (default)/ 512MB |

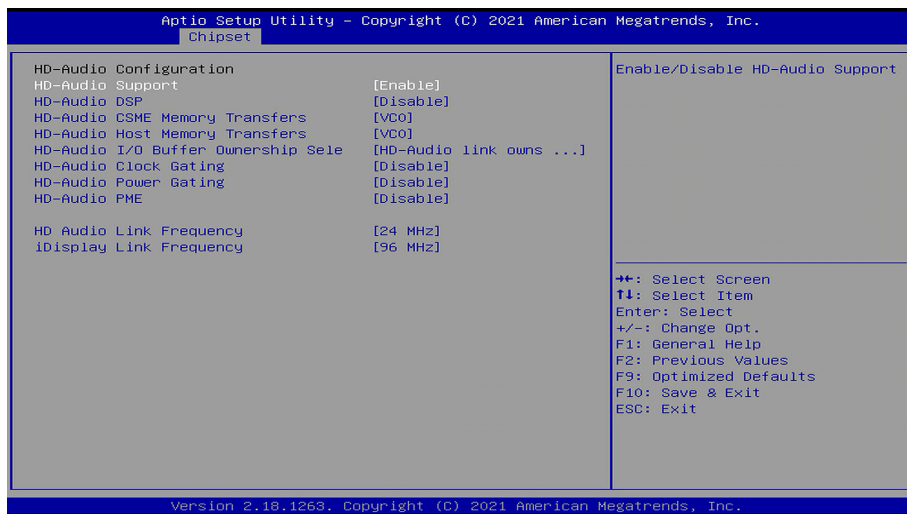
3.3.3 IPU Configuration



The featured settings and delivered info are:

| Item | Description |
|--------------------|---|
| IPU Enable/Disable | Enable/Disable IPU Device ► Options: Enable/Disable (default) |

3.3.4 HD-Audio Configuration

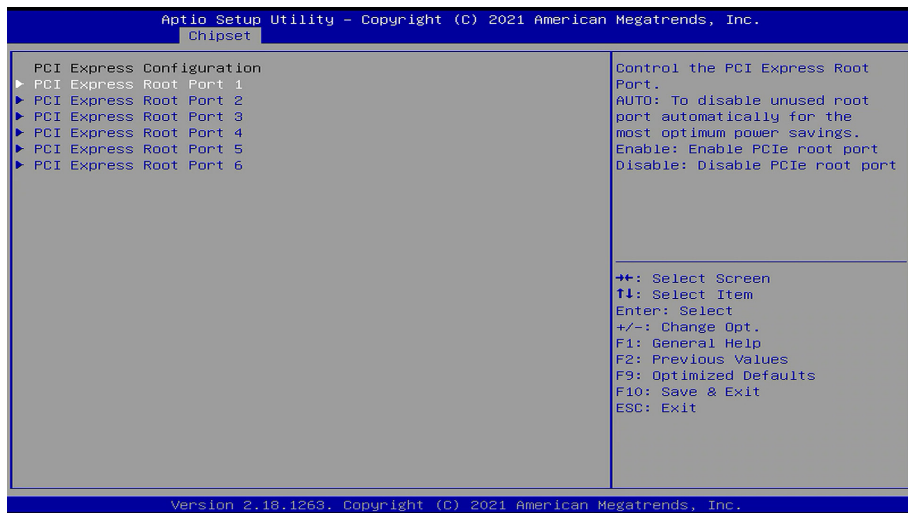


The featured settings and delivered info are:

| Item | Description |
|------------------------------------|---|
| HD-Audio Support | Enable/disable HD-Audio Support. ▶ Options: Disabled and Enabled (default). |
| HD-Audio DSP | Enable/disable HD-Audio DSP Support. ▶ Options: Disabled (default) and Enabled . |
| HD-Audio CSME Memory Transfers | Set HD-Audio CSME Memory Transfers to VCO/VC2. ▶ Options: VC0 (default) and VC2 . |
| HD-Audio Host Memory Transfers | Set HD-Audio Host Memory Transfers to VCO/VC2. ▶ Options: VC0 and VC2 . |
| HD-Audio I/O Buffer Ownership Sele | Set HD-Audio I/O Buffer Ownership. ▶ Options: HD-Audio link owns all the I/O buffers (default) and I2S port owns all the I/O buffers |
| HD-Audio Clock Gating | Enable/Disable HD-Audio Clock Gating ▶ Options: Disabled (default) and Enabled . |
| HD-Audio Power Gating | Enable/Disable HD-Audio Power Gating ▶ Options: Disabled (default) and Enabled . |
| HD-Audio PME | Enable/Disable HD-Audio PME ▶ Options: Disabled (default) and Enabled . |

| | |
|-------------------------|--|
| HD-Audio Link Frequency | Select HD Audio Link frequency. Applicable only if HDA codec supports selected frequency. ▶ Options: 6MHz, 12MHz, 24MHz (default). |
| iDisplay Link Frequency | Select iDisplay Link Frequency. Applicable only if iDisp codec supports selected frequency. ▶ Options: 48MHz, 96MHz (default). |

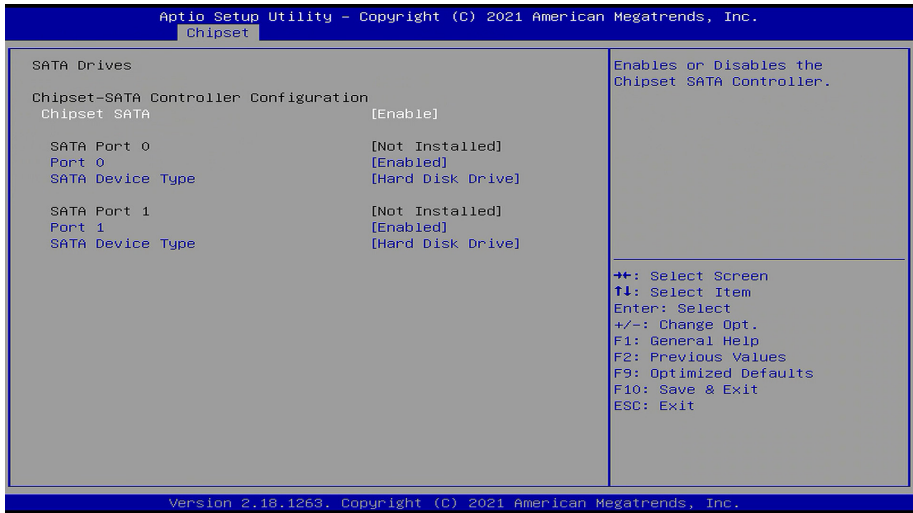
3.3.5 PCI Express Configuration



The featured settings and delivered info are:

| Item | Description |
|-----------------------------------|--|
| PCI Express Root Port 1/2/3/4/5/6 | Control the PCI Express Root Port. <ul style="list-style-type: none"> Options: <ul style="list-style-type: none"> Auto (default): To disable unused root port automatically for the most optimum power savings. Enable: Enable PCIe root port Disable: Disable PCIe root port |
| ASPM | PCI Express Active State Power Management settings. <ul style="list-style-type: none"> Options: Disabled (default), L0s, L1, L0sL1 and Auto |
| PCIe Speed | Configure PCIe Speed. CHV A1 always with Gen1 speed. <ul style="list-style-type: none"> Options: Auto (default), Gen 2 and Gen 1 |

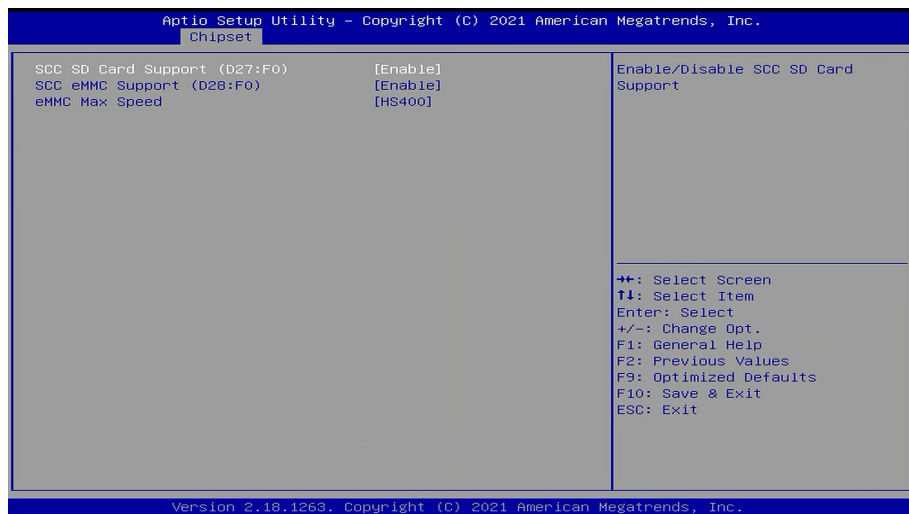
3.3.6 SATA Drives



The featured settings and delivered info are:

| Item | Description |
|------------------|--|
| Chipset SATA | Enables or disables the chipset SATA controller. ▶ Options: Enabled (default) and Disabled |
| Port 0/1 | Enables or disables the SATA port ▶ Options: Enabled (default) and Disabled |
| SATA Device Type | Identify the SATA port is connected to Solid State Drive or Hard Disk Drive. ▶ Options: Hard Disk Drive (default) and Solid State Drive . |

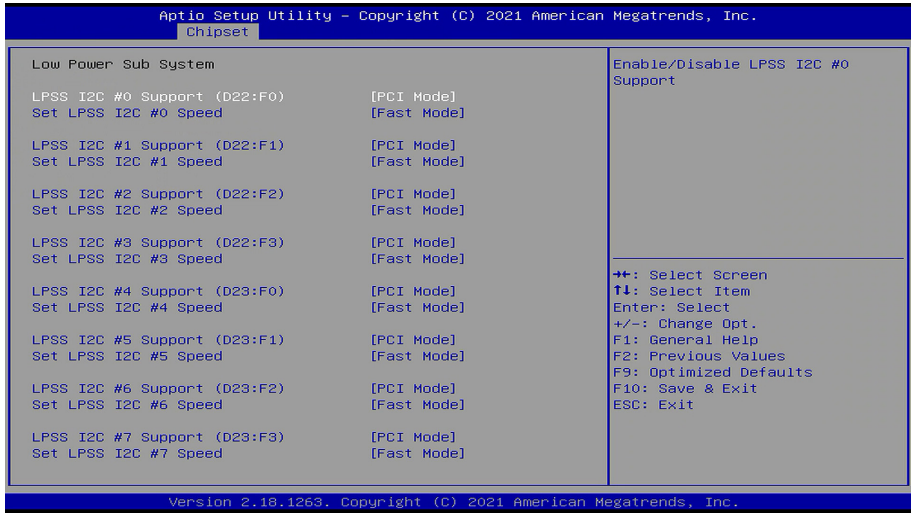
3.3.7 SCC Configuration



The featured settings and delivered info are:

| Item | Description |
|---------------------|--|
| SCC SD Card Support | Enable/Disable SCC SD Card Support. ▶ Options: Disabled and Enabled (default). |
| SCC eMMC Support | Enable/Disable SCC eMMC Support. ▶ Options: Disabled and Enabled (default). |
| eMMC Max Speed | Select the eMMC max Speed allowed. ▶ Options: HS400 (default), HS200 and DDR50 . |

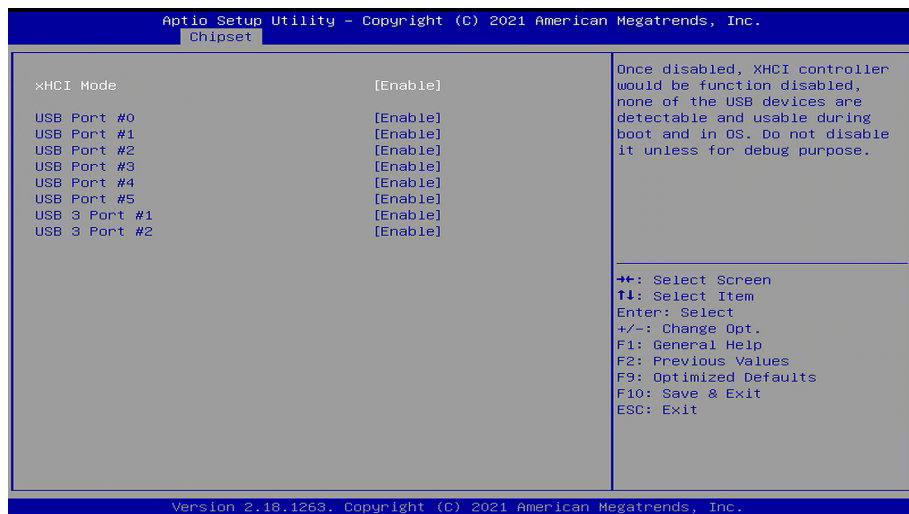
3.3.8 LPSS Configuration



The featured settings and delivered info are:

| Item | Description |
|---------------------------------|---|
| LPSS I ² C Support | Enable/Disable LPSS I ² C (#0~#7) Support. ▶ Options: Disabled (default), PCI Mode and ACPI Mode . |
| Set LPSS I ² C Speed | Select LPSS I ² C (#0~#7) Speed. ▶ Options: Standard , Fast Mode (default) Fast Plus Mode , and High Speed Mode . |

3.3.9 USB Configuration

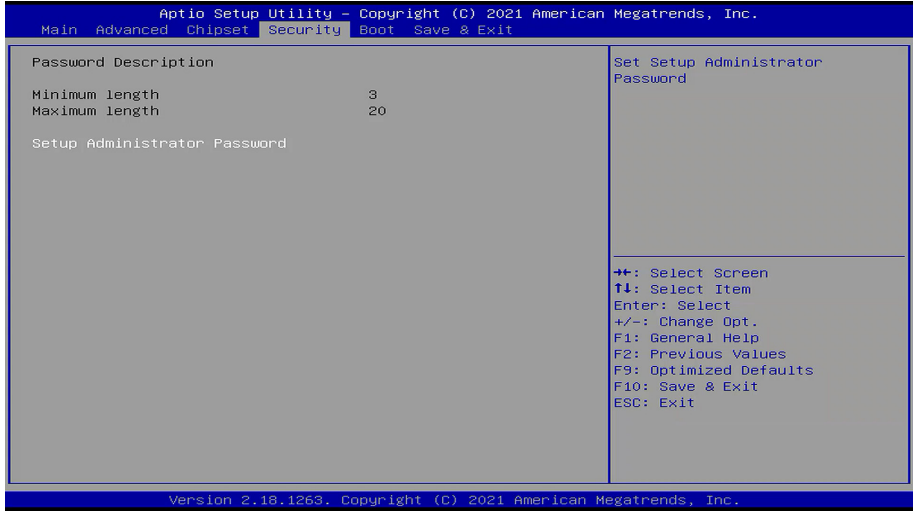


The featured settings and delivered info are:

| Item | Description |
|---------------------------|---|
| XHCI Mode | Enable (default) or Disable XHCI Mode. |
| USB Port Disable Override | Enable/Disable USB Port. Once disabled, any USB devices plug into the connector will not be detected by BIOS or OS. ► Options: Disabled and Enabled (default). |

3.4 Security

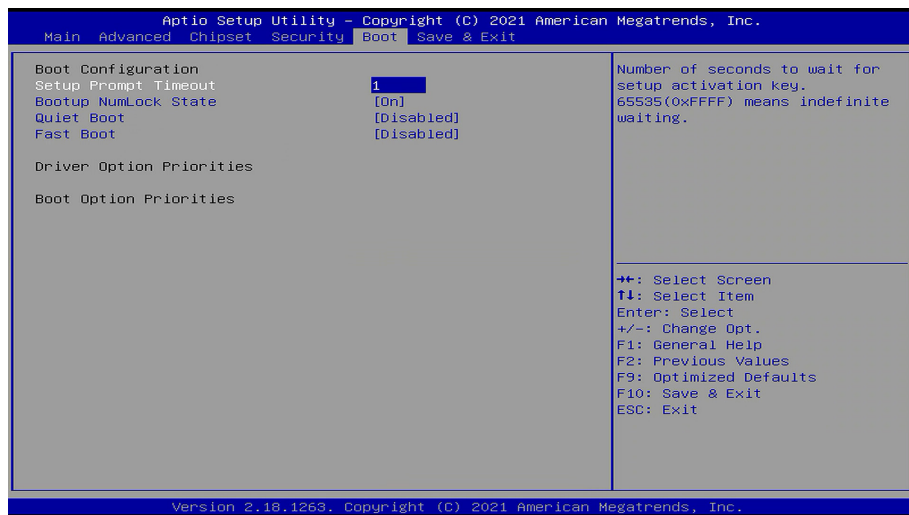
The **Security** menu sets up the administrator password.



The featured settings and delivered info are:

| Setting | Description |
|------------------------|---|
| Administrator Password | <p>To set up an administrator password:</p> <ol style="list-style-type: none"> 1. Select Administrator Password. The screen then pops up an Create New Password dialog. 2. Enter your desired password that is no less than 3 characters and no more than 20 characters. 3. Hit [Enter] key to submit. |

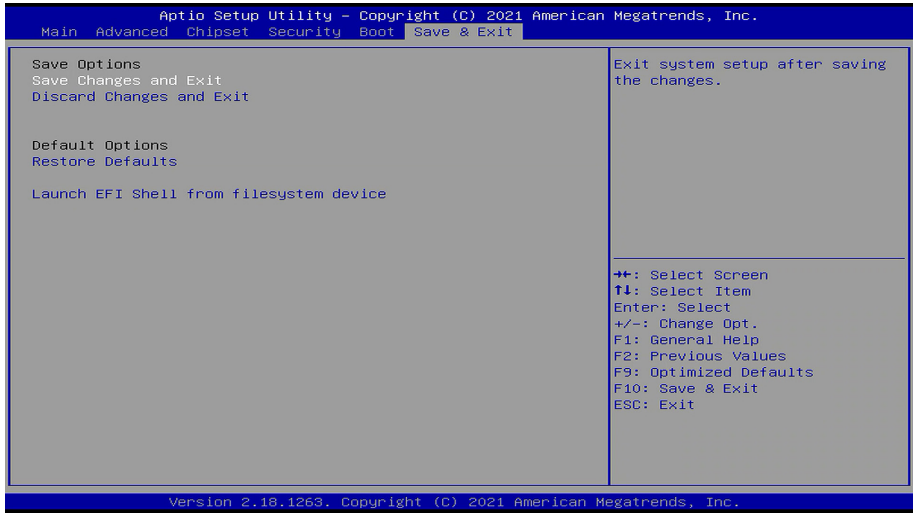
3.5 Boot



The featured settings and delivered info are:

| Setting | Description |
|------------------------|---|
| Setup Prompt Timeout | Number of seconds to wait for setup activation key. 65535(0xFFFF) means indefinite waiting. |
| Boot NumLock State | Select the keyboard NumLock state. ► Options: On (default) and Off . |
| Quiet Boot | Enable (default) or Disable Quiet Boot option. |
| Boot Option Priorities | Sets the boot priority among the available device types. |

3.6 Save & Exit



The featured settings and delivered info are:

| Setting | Description |
|---|---|
| Save Changes and Exit | Exit system setup after saving the changes. ▶ Enter the item and then a dialog box pops up: Save configuration and exit? (Yes/ No) |
| Discard Changes and Exit | Exit system setup without saving the changes. ▶ Enter the item and then a dialog box pops up: Quit without saving? (Yes/ No) |
| Restore Defaults | Restore/Load Default values for all the setup options. ▶ Enter the item and then a dialog box pops up: Load Optimized Defaults? (Yes/ No) |
| Launch EFI Shell from filesystem device | Attempts to launch EFI shell application (Shell.efi) from one of the available filesystem devices. |

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Appendices

Appendix A. I/O Port Address Map

Each peripheral device in the system is assigned a set of I/O port addresses which also becomes the identity of the device.

The following table lists the I/O port addresses used.

| Address | Device Description |
|-----------------------|---|
| 0x000003F8-0x000003FF | Communications Port (CON1) |
| 0x000002F8-0x000002FF | Communications Port (COM1) |
| 0x000003E8-0x000003EF | Communications Port (COM2) |
| 0x000002E8-0x000002EF | Communications Port (COM3) |
| 0x000002F0-0x000002F7 | Communications Port (COM4) |
| 0x0000D000-0x0000D01F | Ethernet Controller |
| 0x0000E000-0x0000E01F | Ethernet Controller |
| 0x00000060-0x00000060 | Microsoft PS/2 Mouse |
| 0x00000064-0x00000064 | Microsoft PS/2 Mouse |
| 0x00000070-0x00000077 | Motherboard resources |
| 0x00000A00-0x00000A0F | Motherboard resources |
| 0x00000A10-0x00000A1F | Motherboard resources |
| 0x00000A20-0x00000A2F | Motherboard resources |
| 0x0000004E-0x0000004F | Motherboard resources |
| 0x00000061-0x00000061 | Motherboard resources |
| 0x00000063-0x00000063 | Motherboard resources |
| 0x00000065-0x00000065 | Motherboard resources |
| 0x00000067-0x00000067 | Motherboard resources |
| 0x00000080-0x0000008F | Motherboard resources |
| 0x00000092-0x00000092 | Motherboard resources |
| 0x000000B2-0x000000B3 | Motherboard resources |
| 0x00000400-0x0000047F | Motherboard resources |
| 0x00000500-0x000005FE | Motherboard resources |
| 0x00000CF8-0x00000CFF | PCI bus |
| 0x00000D00-0x0000FFFF | PCI bus |
| 0x0000D000-0x0000D01F | PCI Express standard Root Port |
| 0x0000E000-0x0000E01F | PCI Express standard Root Port |
| 0x00000020-0x00000021 | Programmable interrupt controller |
| 0x000000A0-0x000000A1 | Programmable interrupt controller |
| 0x000004D0-0x000004D1 | Programmable interrupt controller |
| 0x0000F040-0x0000F05F | SM Bus Controller |
| 0x0000F060-0x0000F07F | Standard AHCI 1.0 Serial ATA controller |
| 0x00000060-0x00000060 | Standard PS/2 Keyboard |
| 0x00000064-0x00000064 | Standard PS/2 Keyboard |
| 0x0000F000-0x0000F03F | Standard VGA Graphics Adapter |
| 0x000003B0-0x000003BB | Standard VGA Graphics Adapter |
| 0x000003C0-0x000003DF | Standard VGA Graphics Adapter |
| 0x00000070-0x00000071 | System CMOS/real time clock |
| 0x00000040-0x00000043 | System timer |
| 0x00000050-0x00000053 | System timer |

Appendix B. Interrupt Request Lines (IRQ)

Peripheral devices use interrupt request lines to notify CPU for the service required. The following table shows the IRQ used by the devices on board.

| Level | Function |
|--------------|---|
| IRQ0 | System timer |
| IRQ1 | Standard PS/2 Keyboard |
| IRQ3 | Communications Port (COM1) |
| IRQ4 | Communications Port (COM1) |
| IRQ5 | Ethernet Controller |
| IRQ5 | Ethernet Controller |
| IRQ5 | SM Bus Controller |
| IRQ5 | PCI Encryption/Decryption Controller |
| IRQ7 | Communications Port (COM4) |
| IRQ10 | Communications Port (COM3) |
| IRQ11 | Communications Port (COM2) |
| IRQ12 | Microsoft PS/2 Mouse |
| IRQ18 | SDA Standard Compliant SD Host Controller |
| IRQ19 | Standard AHCI 1.0 Serial ATA Controller |
| IRQ22 | High Definition Audio Controller |

Appendix C. BIOS Memory Map

| Address | Device Description |
|------------------------|---|
| 0xFF000000-0xFFFFFFFF | Intel(R) 82802 Firmware Hub Device |
| 0x81200000-0x8127FFFF | Ethernet Controller |
| 0x81200000-0x8127FFFF | PCI Express standard Root Port |
| 0x81280000-0x81283FFF | Ethernet Controller |
| 0x8141C000-0x8141C7FF | Standard AHCI 1.0 Serial ATA Controller |
| 0xFED80000-0xFED87FFF | Motherboard resources |
| 0x81300000-0x8137FFFF | Ethernet Controller |
| 0x81300000-0x8137FFFF | PCI Express standard Root Port |
| 0x81380000-0x81383FFF | Ethernet Controller |
| 0x80000000-0x80FFFFFF | Standard VGA Graphics Adapter |
| 0x80000000-0x80FFFFFF | PCI bus |
| 0x90000000-0x9FFFFFFF | Standard VGA Graphics Adapter |
| 0xA0000-0xBFFFF | Standard VGA Graphics Adapter |
| 0xA0000-0xBFFFF | PCI bus |
| 0x81400000-0x8140FFFF | Intel(R) USB 3.0 extensible host controller |
| 0x81410000-0x81413FFF | High Definition Audio Controller |
| 0x81418000-0x8141801F | SM Bus Controller |
| 0xC0000-0xDFFFF | PCI bus |
| 0xE0000-0xFFFFF | PCI bus |
| 0x8141D000-0x8141DFFF | SDA Standard Compliant SD Host Controller |
| 0xE0000000-0xEFFFFFFF | Motherboard resources |
| 0xFEAA0000-0xFEFFFFFF | Motherboard resources |
| 0xFED01000-0xFED01FFF | Motherboard resources |
| 0xFED03000-0xFED03FFF | Motherboard resources |
| 0xFED06000-0xFED06FFF | Motherboard resources |
| 0xFED08000-0xFED09FFF | Motherboard resources |
| 0xFED1C000-0xFED1CFFF | Motherboard resources |
| 0xFEE00000-0xFEEFFFFFF | Motherboard resources |
| 0x8141B000-0x8141BFFF | Motherboard resources |
| 0x81419000-0x81419FFF | Motherboard resources |
| 0x81100000-0x811FFFFFF | PCI Encryption/Decryption Controller |
| 0x81000000-0x810FFFFFF | PCI Encryption/Decryption Controller |

Appendix D: Watchdog Timer (WDT) Setting

WDT is widely used for industry application to monitor the activity of CPU. Application software depends on its requirement to trigger WDT with adequate timer setting. Before WDT time out, the functional normal system will reload the WDT. The WDT never time out for a normal system. The WDT will not be reloaded by an abnormal system, then WDT will time out and reset the system automatically to avoid abnormal operation.

This board supports 255 levels watchdog timer by software programming I/O ports. Below are the source codes written in C, please take them as WDT application example.

```
#include "math.h"
#include "stdio.h"
#include "dos.h"

#define DELAY_TIME 10

#define _SMBBA 0xF040 /* SMBus Base Address */
#define _SMBSA 0x6E /* SMBus Slave Address, 75111R's Add = 6Eh or 9Ch */

unsigned char DIO_Set(unsigned char oMode, unsigned char oData);
unsigned char SMB_Byte_READ(int SMPORT, int DeviceID, int iREG_INDEX);
void SMB_Byte_WRITE(int SMPORT, int DeviceID, int oREG_INDEX, int oREG_DATA);

void main()
{
    WDT_Start(10);

    while(1)
    {
        iCount = WDT_Count();
        printf("\r Counts : %d ",iCount);

        delay(1000);
    }
}

void WDT_Start(int iCount)
{
    int iData;

    /* Configuration and function select Register - Enable WDTOUT2# output */
    iData = SMB_Byte_READ(SMB_PORT_AD,SMB_DEVICE_ADD,0x03);
    iData = iData | 0x03;
    SMB_Byte_WRITE(SMB_PORT_AD,SMB_DEVICE_ADD,0x03,iData);
    delay(DELAY_TIME);

    /* Watchdog Timer Range Register */
    SMB_Byte_WRITE(SMB_PORT_AD,SMB_DEVICE_ADD,0x37,iCount);
}
```

```
    delay(DELAY_TIME);

    /* Watchdog Timer Control Register */
    SMB_Byte_WRITE(SMB_PORT_AD, SMB_DEVICE_ADD, 0x36, 0x72);
}

int WDT_Count(void)
{
    int iData;

    /* Watchdog Timer Range Register */
    iData = SMB_Byte_READ(SMB_PORT_AD, SMB_DEVICE_ADD, 0x37);

    return iData;
}

void WDT_Clear(int iCount)
{
    /* Watchdog Timer Range Register */
    SMB_Byte_WRITE(SMB_PORT_AD, SMB_DEVICE_ADD, 0x37, iCount);
}

void WDT_Stop(void)
{
    /* Watchdog Timer Control Register */
    SMB_Byte_WRITE(SMB_PORT_AD, SMB_DEVICE_ADD, 0x36, 0x52);
}
```