HiCORE-i89Q1
HiCORE-i89Q2

PICMG 1.0 Full size SBC

User's Manual

Version 1.2

2018.01

Revision History

Version	Release Time	Description
1.0	2017.06	Initial release
1.1	2017.06	Add cable kit to 1.1 Packing List
1.2	2018.01	• Modify audio descripton in 1.4 Specifications • Add FCDB-1111 to optional accessories in 1.2 Ordering Information • Modify Audio 1 pin header description in bock diagram

Contents

Preface

Copyright Notice

The information in this document is subject to change without prior notice in order to improve the reliability, design and function. It does not represent a commitment on the part of the manufacturer.

Under no circumstances will the manufacturer be liable for any direct, indirect, special, incidental, or consequential damages arising from the use or inability to use the product or documentation, even if advised of the possibility of such damages.

Declaration of Conformity

CE

The CE symbol on your product indicates that it is in compliance with the directives of the Union European (EU). A Certificate of Compliance is available by contacting Technical Support.

This product has passed the CE test for environmental specifications when shielded cables are used for external wiring. We recommend the use of shielded cables. This kind of cable is available from ARBOR. Please contact your local supplier for ordering information.

This product has passed the CE test for environmental specifications. Test conditions for passing included the equipment being operated within an industrial enclosure. In order to protect the product from being damaged by ESD (Electrostatic Discharge) and EMI leakage, we strongly recommend the use of CE-compliant industrial enclosure products.

Warning

This is a class A product. In a domestic environment this product may cause radio interference in which case the user may be required to take adequate measures.

FCC Class A

This device complies with Part 15 of the FCC Rules. Operation is subject to the following two conditions:

(1)This device may not cause harmful interference, and

(2)This device must accept any interference received, including interference that may cause undesired operation.

NOTE:

This equipment has been tested and found to comply with the limits for a Class A digital device, pursuant to Part 15 of the FCC Rules. These limits are designed to provide reasonable protection against harmful interference when the equipment is operated in a commercial environment. This equipment generates, uses, and can radiate radio frequency energy and, if not installed and used in accordance with the instruction manual, may cause harmful interference to radio communications. Operation of this equipment in a residential area is likely to cause harmful interference in which case the user will be required to correct the interference at his own expense.

RoHS

ARBOR Technology Corp. certifies that all components in its products are in compliance and conform to the European Union's Restriction of Use of Hazardous Substances in Electrical and Electronic Equipment (RoHS) Directive 2002/95/EC.

The above mentioned directive was published on 2/13/2003. The main purpose of the directive is to prohibit the use of lead, mercury, cadmium, hexavalent chromium, polybrominated biphenyls (PBB), and polybrominated diphenyl ethers (PBDE) in electrical and electronic products. Member states of the EU are to enforce by 7/1/2006.

ARBOR Technology Corp. hereby states that the listed products do not contain unintentional additions of lead, mercury, hex chrome, PBB or PBDB that exceed a maximum concentration value of 0.1% by weight or for cadmium exceed 0.01% by weight, per homogenous material. Homogenous material is defined as a substance or mixture of substances with uniform composition (such as solders, resins, plating, etc.). Lead-free solder is used for all terminations (Sn(96-96.5%), Ag(3.0-3.5%) and Cu(0.5%)).

SVHC / REACH

To minimize the environmental impact and take more responsibility to the earth we live, Arbor hereby confirms all products comply with the restriction

of SVHC (Substances of Very High Concern) in (EC) 1907/2006 (REACH --Registration, Evaluation, Authorization, and Restriction of Chemicals) regulated by the European Union.

All substances listed in SVHC < 0.1 % by weight (1000 ppm)

About This User's Manual

This user's manual provides general information and installation instructions about the product. This User's Manual is intended for experienced users and integrators with hardware knowledge of personal computers. If you are not sure about any description in this booklet. Please consult your vendor before further handling.

Warning

Single Board Computers and their components contain very delicate Integrated Circuits (IC). To protect the Single Board Computer and its components against damage from static electricity, you should always follow the following precautions when handling it :

1. Disconnect your Single Board Computer from the power source when you want to work on the inside.
2. Hold the board by the edges and try not to touch the IC chips, leads or circuitry.
3. Use a grounded wrist strap when handling computer components.
4. Place components on a grounded antistatic pad or on the bag that comes with the Single Board Computer, whenever components are separated from the system.

Replacing the Lithium Battery

Incorrect replacement of the lithium battery may lead to a risk of explosion.

The lithium battery must be replaced with an identical battery or a battery type recommended by the manufacturer.

Do not throw lithium batteries into the trash-can. It must be disposed of in accordance with local regulations concerning special waste.

Technical Support

If you have any technical difficulties, please do not hesitate to call or e-mail our customer service.

http://www.arbor-technology.com

E-mail:info@arbor.com.tw

Warranty

This product is warranted to be in good working order for a period of two years from the date of purchase. Should this product fail to be in good working order at any time during this period, we will, at our option, replace or repair it at no additional charge except as set forth in the following terms. This warranty does not apply to products damaged by misuse, modifications, accident or disaster.

Vendor assumes no liability for any damages, lost profits, lost savings or any other incidental or consequential damage resulting from the use, misuse of, or inability to use this product. Vendor will not be liable for any claim made by any other related party.

Vendors disclaim all other warranties, either expressed or implied, including but not limited to implied warranties of merchantability and fitness for a particular purpose, with respect to the hardware, the accompanying product's manual(s) and written materials, and any accompanying hardware. This limited warranty gives you specific legal rights.

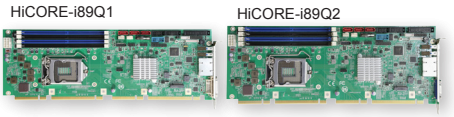
Return authorization must be obtained from the vendor before returned merchandise will be accepted. Authorization can be obtained by calling or faxing the vendor and requesting a Return Merchandise Authorization (RMA) number. Returned goods should always be accompanied by a clear problem description.

Chapter 1

Introduction

1.1. Packing List

Before starting with the installation, make sure the following items are shipped. If any item appears damaged or is missing, contact your vendor immediately:

	1 x HiCORE-i89Q1 or HiCORE-i89Q2 PICMG 1.3 Full-size SBC
	1 x Driver CD 1 x Quick Installation Guide
CBK-08-89Q1-00	Cable Kit 1 x RS-232 cable 1 x RS-232/422/485 cable 3 x SATA cable 2 x USB cable w/ bracket 1 x Keyboard & Mouse cable

1.2. Ordering Information

HiCORE-i89Q1-D-x4	Socket LGA1151/PCH Q170 for 6th Generation Intel® Core™ i7/ i5/ i3 processors PICMG 1.3 full size SBC with BIOS for 1 x PCIe x4 w/ DVI-I
HiCORE-i89Q1-D-x1	Socket LGA1151/PCH Q170 for 6th Generation Intel® Core™ i7/ i5/ i3 processors PICMG 1.3 full size SBC with BIOS for 4 x PCIe x1 w/ DVI-I
HiCORE-i89Q2-V-x4	Socket LGA1151/PCH Q170 for 6th Generation Intel® Core™ i7/ i5/ i3 processors PICMG 1.3 full size SBC with BIOS for 1 x PCIe x4 w/ VGA
HiCORE-i89Q2-V-x1	Socket LGA1151/PCH Q170 for 6th Generation Intel® Core™ i7/ i5/ i3 processors PICMG 1.3 full size SBC with BIOS for 4 x PCIe x1 w/ VGA

Optional Accessories

PBPE-07SA	7-slot PICMG 1.3 backplane
PBPE-13SA	13-slot PICMG 1.3 backplane
PBPE-10SA (OEM request)	10-slot PICMG 1.3 backplane
HS-89Q1-C1	Copper CPU cooler for Intel® Core™ processor series
DP Cable	Male DP port to female DP port cable
FCDB-1111	Realtek ALC888 HD Audio daughterboard

Recommended CPU List

i7-6700 Quad-Core 3.4GHz
i5-6500 Quad-Core 3.6GHz
i3-6100 Dual-Core 3.7GHz

1.3. The Installation Paths of CD Driver

The CPU board supports Windows 10 64-bit. Find the necessary drivers by the following paths on the CD that comes with your purchase.

Windows 10 64-bit

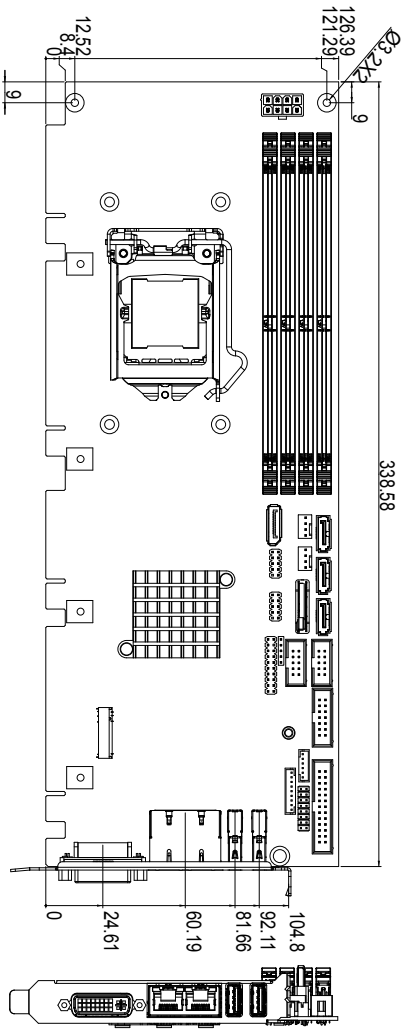
Chipset	\i89X\Chipset\Chipset_10.1.1.13_Public
Audio	\i89X\Audio\7687_PG436_Win10_Win8.1_Win8_Win7_WHQLx64
LAN	\i89X\Ethernet
Graphic	\i89X\Graphic\IntelR Graphics Driver Production Version 15.40.16.64.4364
ME	\i89X\ME\Intel(R)_ME_11.0_Corporate_11.0.0.1202
RAID	\i89X\RAID\Intel Rapid Storage Technology Driver 14.8.0.1042
USB3.0	\i89X\USB3.0\win8.1 64bit\Intel_USB_3.0_xHC_Adaptation_Driver_MR1_Release_1.0.1.45_PV

1.4. Specifications

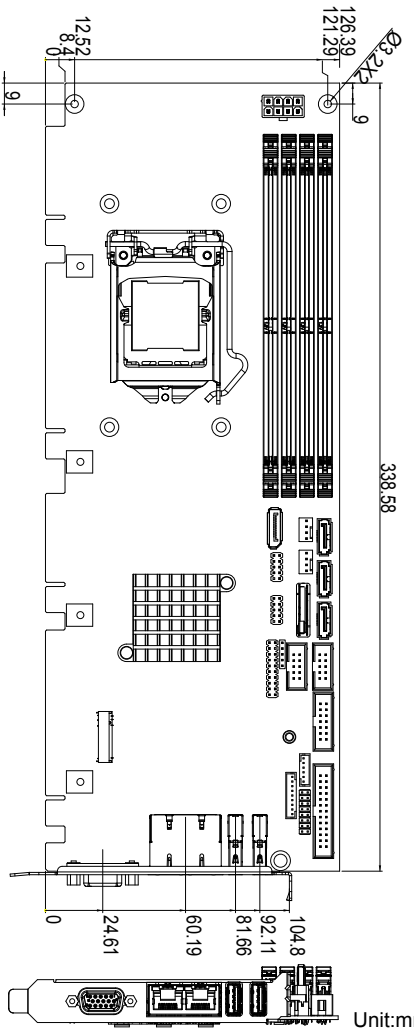
Form Factor	PICMG 1.3 Full-size SBC
CPU	Support 6th Generation Intel® Core™ i7/i5/i3 processors in LGA1151 socket
Chipset	Intel® PCH Q170
Memory	4 x 288-pin DDR4 Long-DIMM sockets, supporting 2133/1866MHz SDRAM up to 64GB
BIOS	AMI UEFI BIOS
Watchdog Timer	1~255 levels reset
Super I/O	Fintek F81768
USB Port	4 x USB 2.0 ports to Golden finger 4 x USB 2.0 ports w/ pin-header 2 x USB 3.0/2.0 ports on bracket
Serial Port	1 x RS-232
	1 x RS-232/422/485 selectable
Expansion Bus	1 x PCIex4 Lanes (HiCORE-i89Q1) or 4 x PCIex1 Lanes (HiCORE-i89Q2) 1 x PCIex16 lanes Gen. 3 4 x PCI masters LPC interface
Storage	Six Serial ATA ports with 600MB/s HDD transfer rate - 3 ports on board - 1 port to NGFF M.2 socket-M - 2 port to Golden finger
	SATA RAID 0, 1, 5, 10 supported
Ethernet Chipset	1 x Intel® i219LM PCIe GbE PHY 1 x Intel® i210AT PCIe GbE controller
Audio Interface	One 1x9-pin wafer connector for HD Audio daughterboard
Digital I/O	8-bit programmable digital input/output
KB/MS	6-pin wafer connector for keyboard and mouse via Y-cable
Parallel Port	SPP/EPP/ECP mode selectable

Graphic Chipset	Integrated Intel® HD Graphics (depends on CPU)
Graphic Interface	1 x DVI-I port on board (HiCORE-i89Q1) or 1 x VGA port on board (HiCORE-i89Q2)
	1 x DisplayPort
OS Support	
Windows 10 64-bit Linux: Ubuntu	
Power Input	DC 12V, 5V
Power Consumption	2.66A@12V
Operating Temp.	0 ~ 60°C (32 ~ 122°F)
Operating Humidity	10 ~ 95% @ 60°C (non-condensing)
Dimensions (L x W)	338 x 126 mm (13.3" x 4.96")

1.6. Board Dimensions



HiCORE-i89Q1



HiCORE-i89Q2

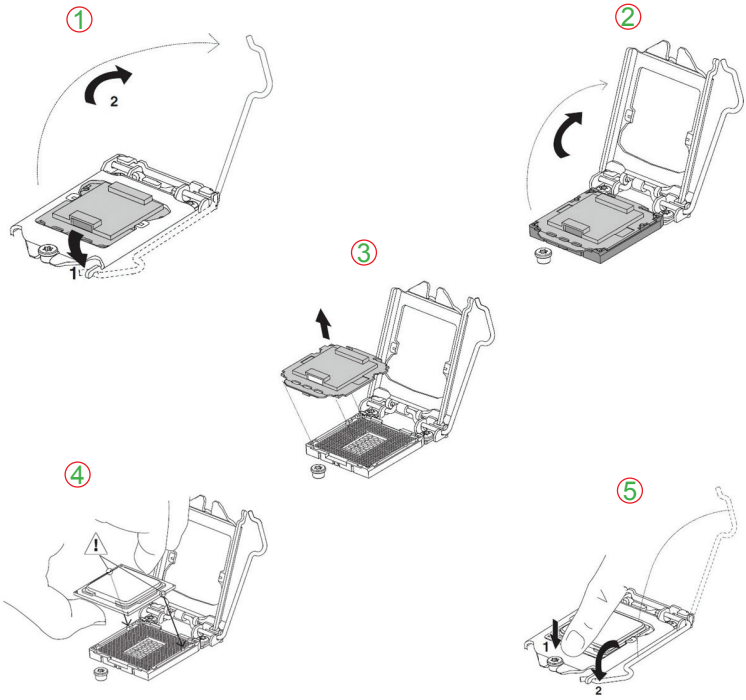
Unit:mm

* The graphic interface depends on your model. The figure is using HiCore-i89Q1's DVI port as an example.

1.7. Installing the CPU

The LGA1151 processor socket comes with a lever to secure the processor. Please refer to the pictures step by step as below.

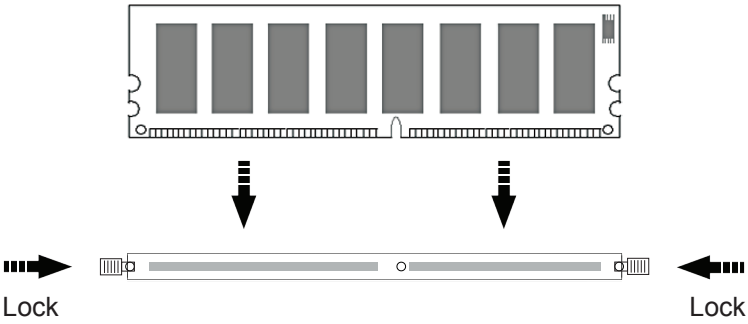
1. Push the lever down to unclip it and lift it.
2. Open the load plate.
3. Remove the protective cover from the load plate. Do not discard the protective cover. Always replace the socket cover if the processor is removed from the socket.
4. Hold processor with your thumb and index fingers, oriented as shown. Ensure your fingers align to the socket cutouts. Align the notches with the socket. Lower the processor straight down without tilting or sliding the processor in the socket.
5. Close the load plate. Pressing down on the load plate, close and engage the socket lever.



1.8. Installing the Memory

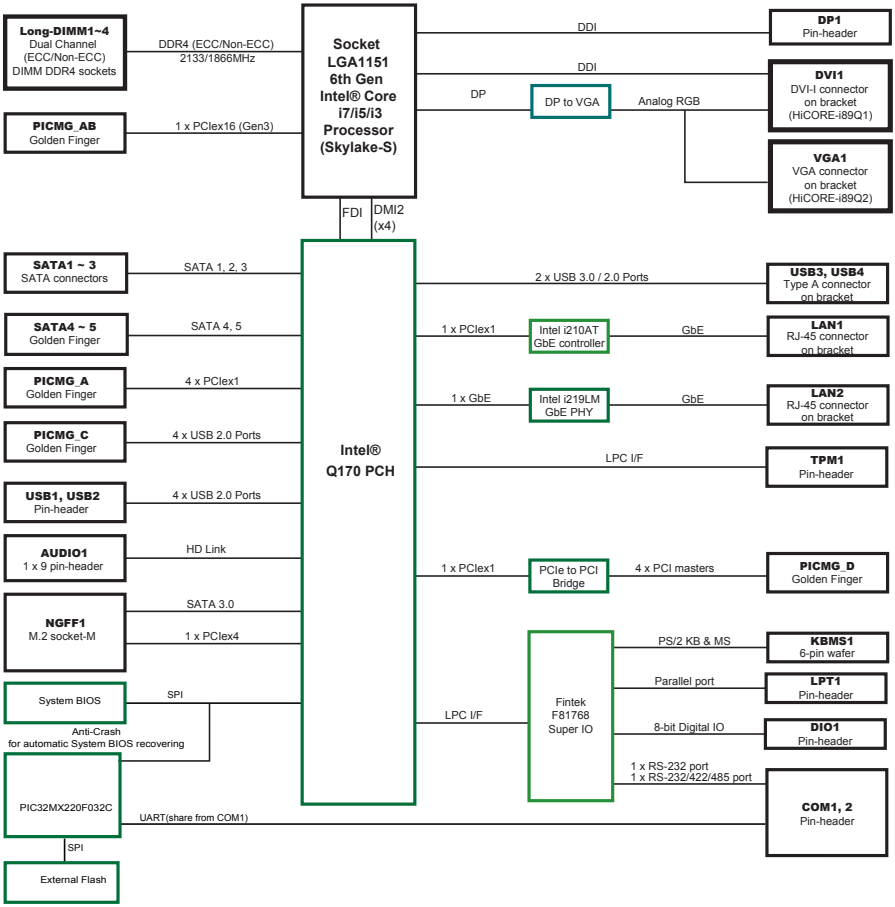
To install the Memory module, locate the Memory DIMM slot on the board and perform as below:

1. Hold the Memory module so that the key of the Memory module align with those on the Memory DIMM slot.
2. Gently push the Memory module in an upright position and a right way until the clips of the DIMM slot close to lock the Memory module in place, when the Memory module touches the bottom of the DIMM slot.
3. To remove the Memory module, just pressing the clips of DIMM slot with both hands.



Chapter 2
Installation

2.1. Block Diagram



2.2. Jumpers & Connectors

2.2.1. Quick Reference

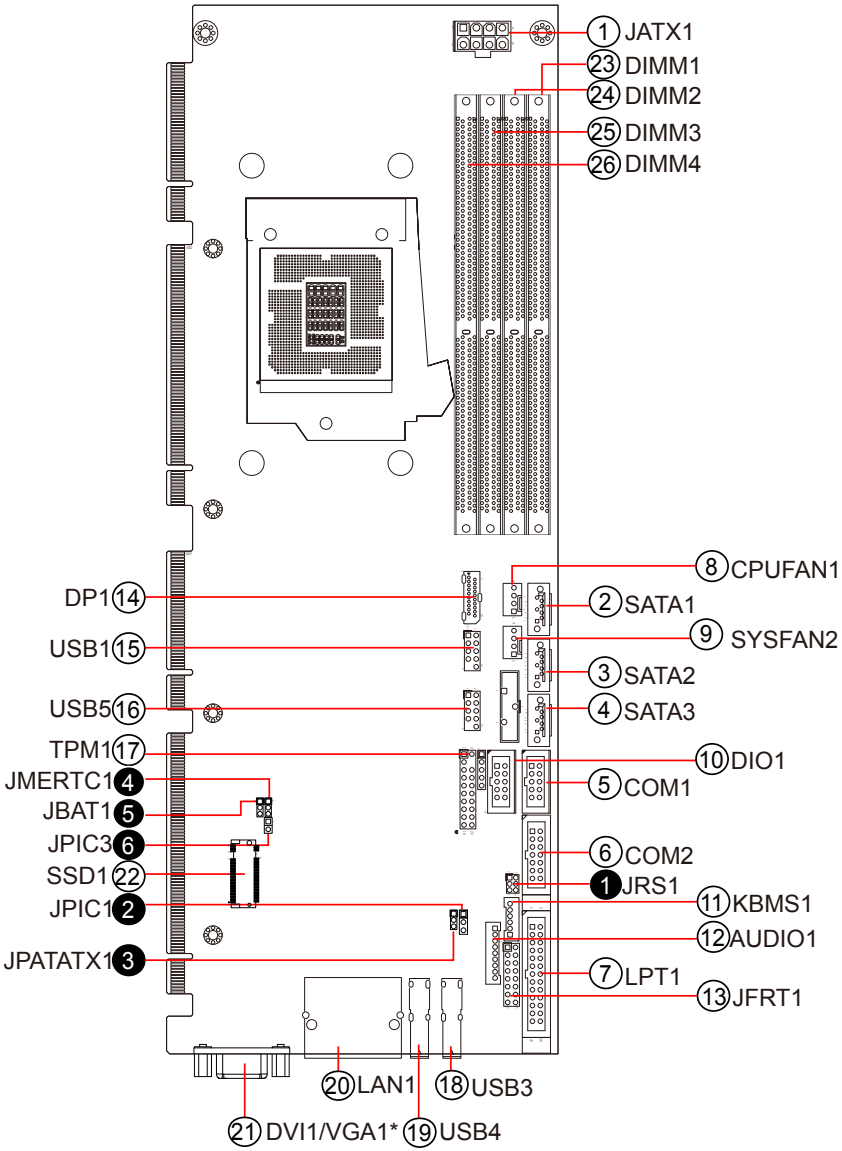
Jumpers

Label	Description
❶JRS1	COM2 RS-232 / 422 / 485 Selection
❷JPIC1	Internal Use
❸JPATATX1	AT/ATX Mode Selection
❹JMERTC1	SRTC Reset Selection
❺JBAT1	CMOS Setting
❻JPIC3	ACT Function Setting

Connectors

Label	Description
①JATX1	ATX 12V Connector
②③④SATA1~3	Serial ATA Connectors
⑤COM1	RS-232 COM Port Connector
⑥COM2	RS-232/422/485 Selectable COM Port Connector
⑦LPT1	Parallel Port Connector
⑧CPUFAN1, ⑨SYSFAN2	Fan Connectors
⑩DIO1	Digital I/O Connector
⑪KBMS1	Keyboard & Mouse Connector
⑫AUDIO1	AUDIO Connector
⑬JFRT1	Switches and Indicators
⑭DP1	DisplayPort Connector
⑮⑯USB1, 5	USB2.0 Connector
⑰TPM1	TPM Connector
⑱⑲USB3, 4	USB 3.0/2.0 Connector
⑳LAN1	Ethernet Connectors
㉑DVI1/ VGA1	DVI-I/ VGA Connector
㉒SSD1	NGFF M-Key Socket
㉓㉔㉕㉖ DIMM1, 2, 3, 4	4x288-pin DDR4 Memory Slots

2.2.2. Jumpers & Connectors Location



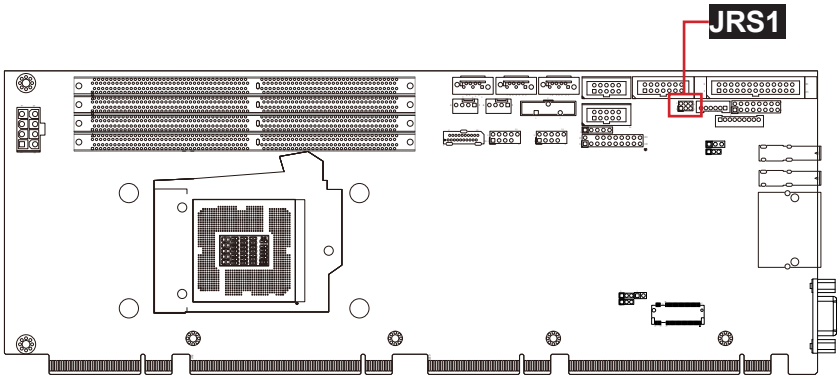
* The graphic interface depends on your model. The figure is using HiCore-i89Q1's DVI port as an example.

2.2.3. Jumpers

❶JRS1

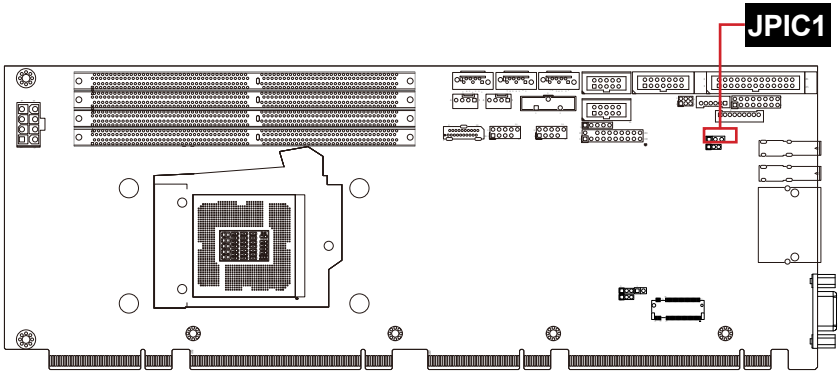
Function: COM2 RS-232 / 422 / 485 Selection
Connector type: 2.00mm pitch 3x2-pin headers

Mode	RS-232 (Default)	RS-422	RS-485
1-2	Short	Open	Open
3-4	Open	Short	Open
5-6	Open	Open	Short
			



❷JPIC1

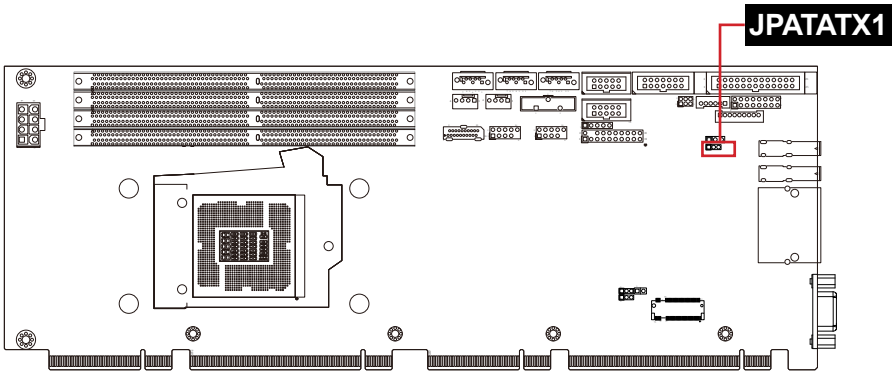
Function: Internal Use
Connector type: 2.00 mm pitch 1x2-pin headers



❸JPATAX1

Function: AT/ATX Mode Selection
Connector type: 2.00mm pitch 1x3-pin headers.

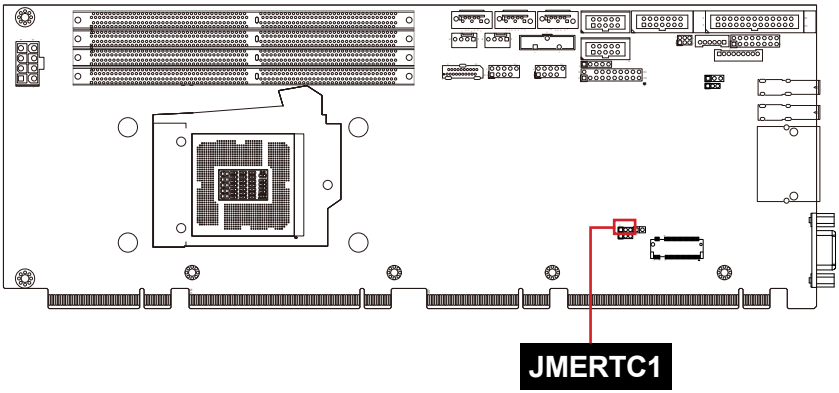
Pin	Mode	
1-2	AT Mode	
2-3	ATX Mode (default)	



❹JMERTC1

Function: SRTC Reset Selection
Connector type: 2.00mm pitch 1×3-pin headers

Pin	Mode	
1-2	Normal (default)	
2-3	Clear ME RTC	



❺JBAT1

Function: CMOS Setting
Connector type: 2.00mm pitch 1x3-pin headers

Pin	Mode	
1-2	Keep CMOS (Default)	
2-3	Clear CMOS	

You may need to clear the CMOS if your system cannot boot up because you forgot your password, the CPU clock setup is incorrect, or the CMOS settings need to be reset to default values after the system BIOS has been updated. Refer to the following solutions to reset your CMOS setting:

Solution A:

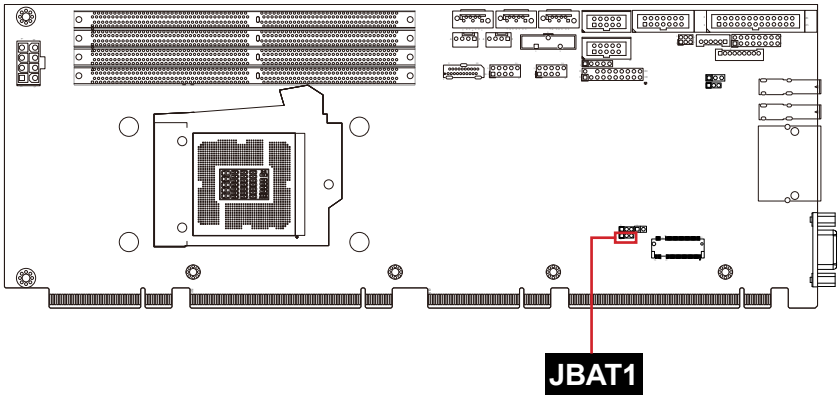
1. Power off the system and disconnect the power cable.
2. Place a shunt to short pin 2 and pin 3 of JBAT1 for five seconds.
3. Place the shunt back to pin 1 and pin 2 of JBAT1.
4. Power on the system.

Solution B:

If the CPU Clock setup is incorrect, you may not be able to boot up. In this case, follow these instructions:

1. Turn the system off, then on again. The CPU will automatically boot up using standard parameters.
2. As the system boots, enter BIOS and set up the CPU clock.

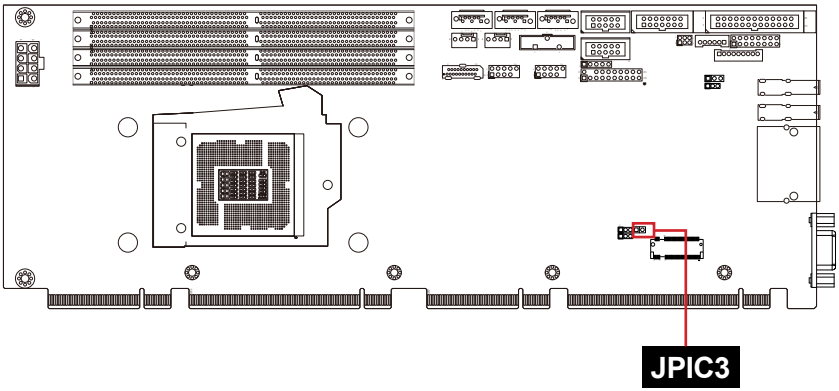
Note: If you are unable to enter BIOS setup, turn the system on and off a few times.



⑥JPIC3

Function: ACT Function Setting
Connector type: 2.00mm pitch 1x3-pin headers

Pin	Mode	
1-2	ACT Enabled (default)	
2-3	ACT Disabled	

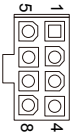


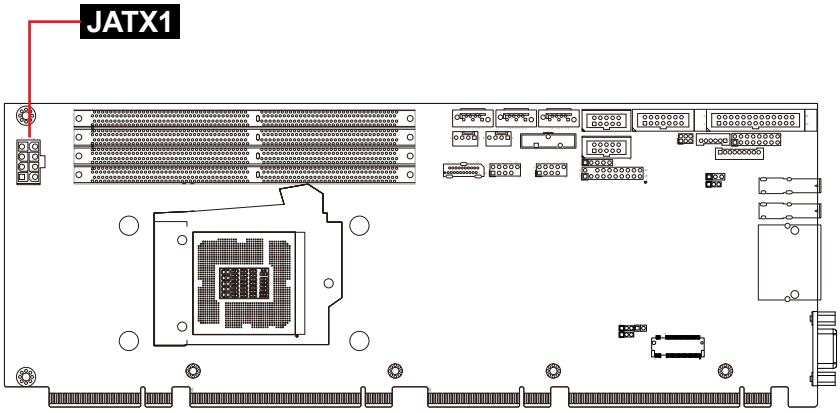
2.2.4. Connectors

①JATX1

Function: ATX 12V Connector
Connector type: 8-pin power connector

Pin	Desc.	Pin	Desc.
1	GND	5	+12V
2	GND	6	+12V-
3	GND	7	+12V
4	GND	8	+12V

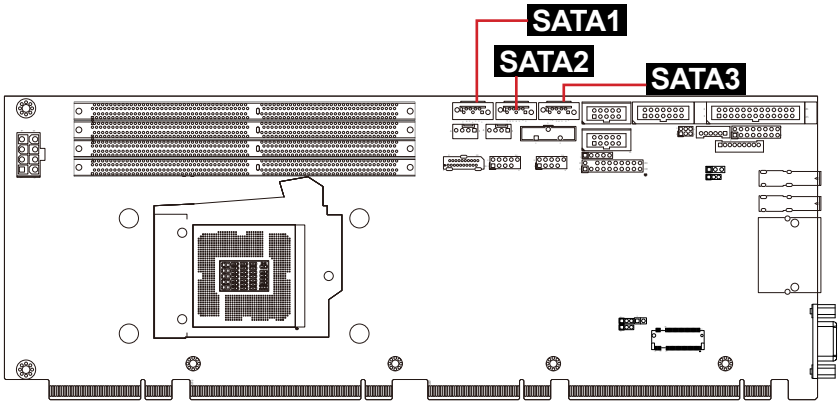




②③④SATA1~3

Function: Serial ATA Connectors

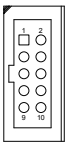
The pin assignments conform to the industry standard.

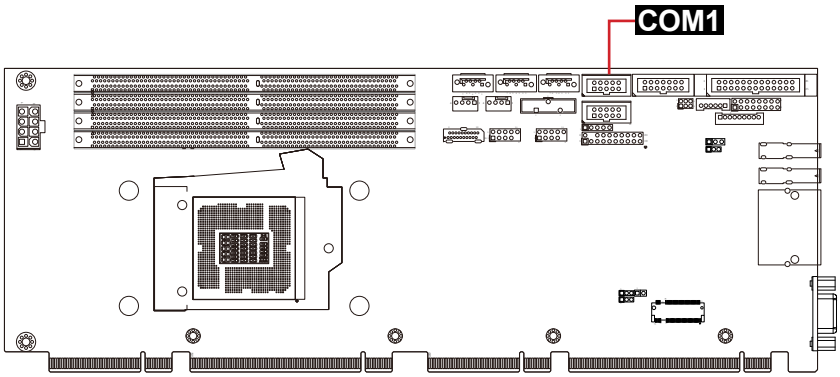


⑤COM1

Function: RS-232 COM Port Connector
Connector Type: 2.54mm pitch 2x5-pin box headers

Pin	Desc.	Pin	Desc.
1	DCD#	2	DSR#
3	RXD	4	RTS#
5	TXD	6	CTS#
7	DTR#	8	RI#
9	GND	10	GND

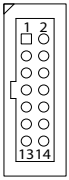


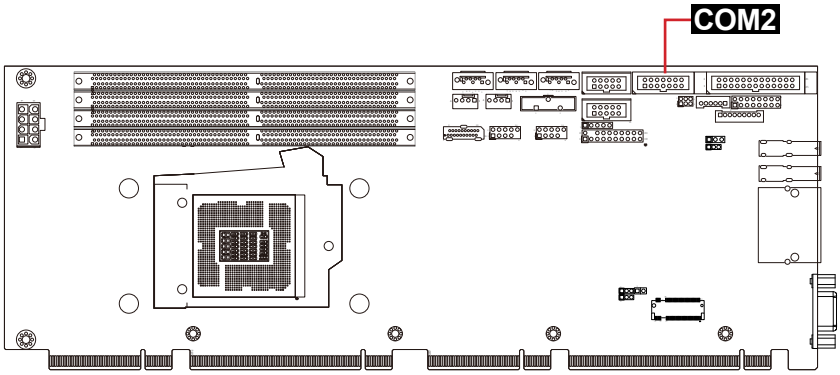


⑥COM2

Function: RS-232/422/485 selectable COM Port Connector
Connector type: 2.54mm pitch 2x7-pin box headers

Pin	Desc.	Pin	Desc.
1	DCD#	2	DSR#
3	RXD	4	RTS#
5	TXD	6	CTS#
7	DTR#	8	RI#
9	GND	10	GND
11	442TX+/ 485+	12	422TX-/ 485-
13	422RX+	14	422RX-

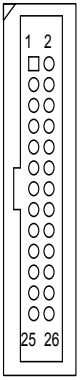


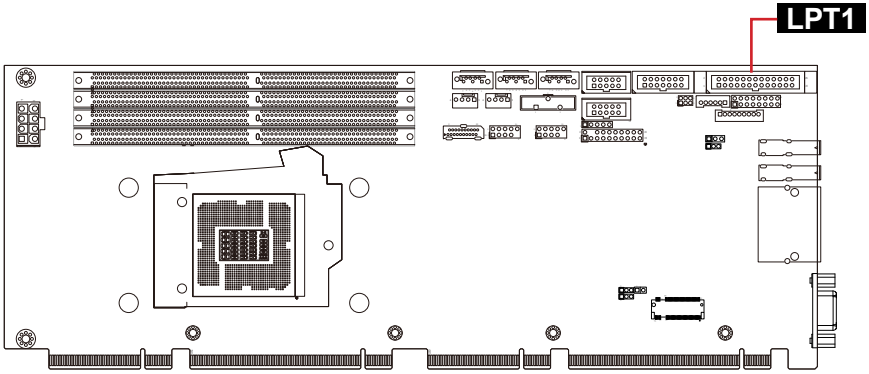


⑦LPT1

Function: Parallel Port Connector
Connector type: 2.54mm pitch 2x13-pin box headers

Pin	Description	Pin	Description
1	LPT_STB#	2	LPT_AFD#
3	LPT_PD0	4	ERR#
5	LPT_PD1	6	LPT_INIT#
7	LPT_PD2	8	LPT_SLIN#
9	LPT_PD3	10	GND
11	LPT_PD4	12	GND
13	LPT_PD5	14	GND
15	LPT_PD6	16	GND
17	LPT_PD7	18	GND
19	ACK#	20	GND
21	BUSY	22	GND
23	PE	24	GND
25	SELECT	26	N/C

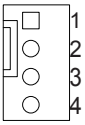


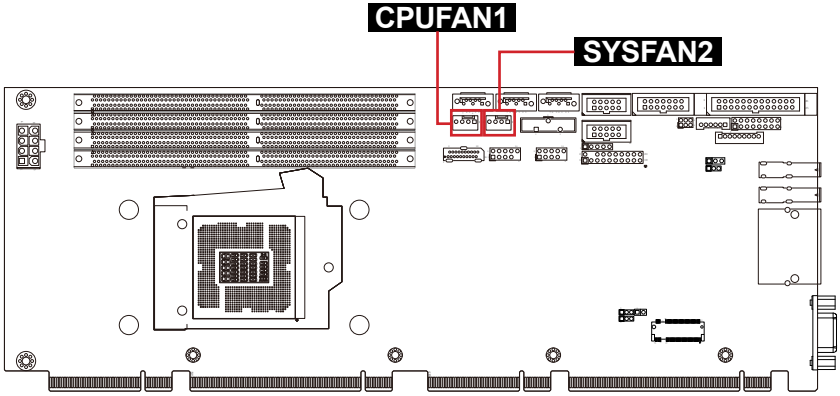


⑧⑨CPUFAN1, SYSFAN2

Function: Fan Connectors
Connector type: 2.54mm pitch 1x4-pin wafer headers

Pin	Description
1	GND
2	+12V
3	RPM
4	CTRL

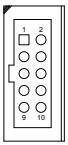


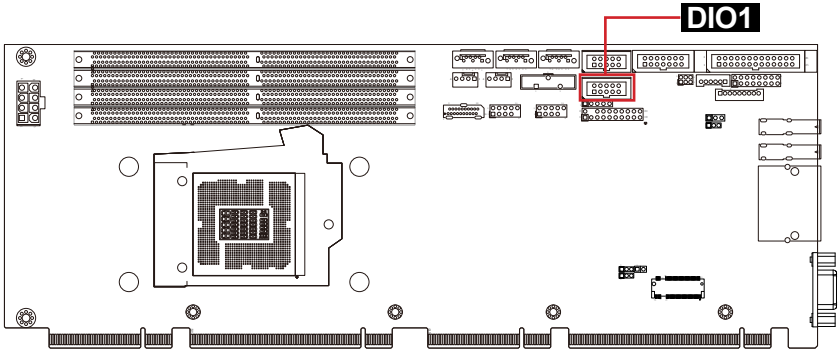


⑩DIO1

Function: Digital I/O Connector
Connector type: 2.54mm pitch 2x5-pin headers

Pin	Desc.	Pin	Desc.
1	DIO0	2	DIO1
3	DIO2	4	DIO3
5	DIO4	6	DIO5
7	DIO6	8	DIO7
9	+V5S	10	GND

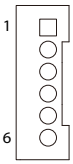


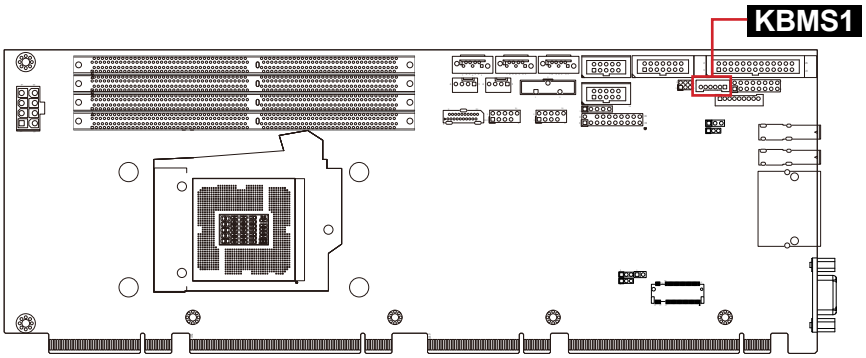


⑪KBMS1

Function: Keyboard & Mouse Connector
Connector type: 2.00mm pitch 1x6-pin wafer headers

Pin	Description
1	KB_DAT
2	GND
3	MS_DAT
4	KB_CLK
5	VCC PS2
6	MS_CLK

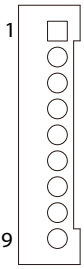


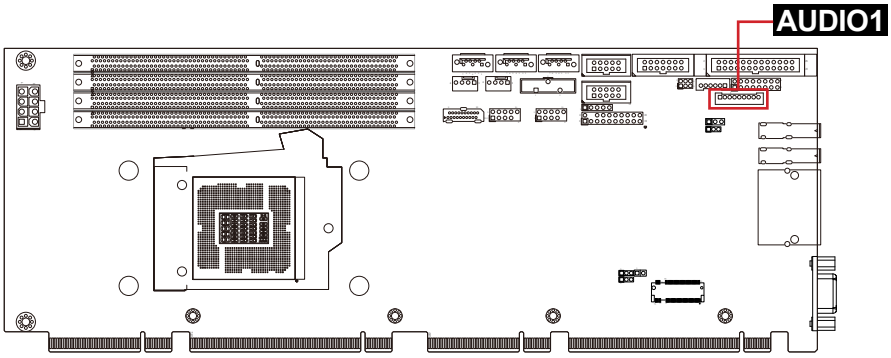


⑫AUDIO1

Function: Audio Connector
Connector type: 2.00mm pitch 1x9-pin headers.

Pin	Desc.
1	+12V
2	+V3.3S
3	HDA_SYNC
4	HDA_SDO
5	GND
6	HDA_BGLK
7	GND
8	HDA_RST#
9	AZA_SDI_0

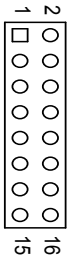


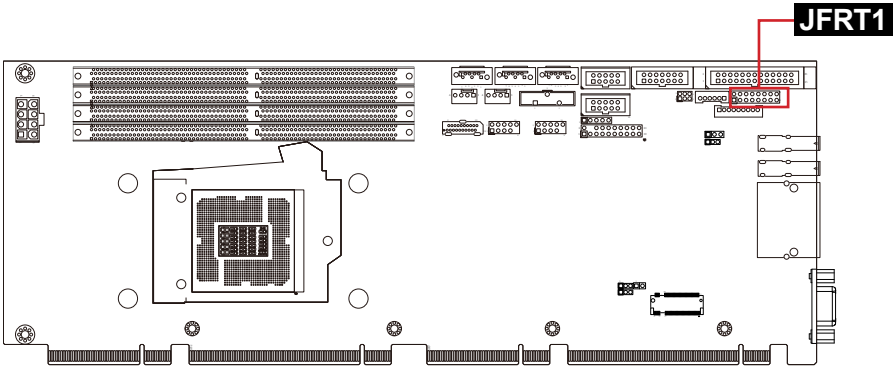


⑬JFRT1

Function: Switches and Indicators
Connector type: 2.54 mm pitch 2x8-pin headers

Pin	Desc.	Pin	Desc.
1	PLED+	2	SW_ON_R_N
3	PLED-	4	GND
5	PLED-	6	EXTRST_N
7	HD_LED_+	8	GND
9	HD_LED_N	10	SPKRV+
11	SMB_CLK_RESUME	12	SPKRV+
13	SMB_DAT_RESUME	14	SPKRV-
15	GND	16	SPKRV-

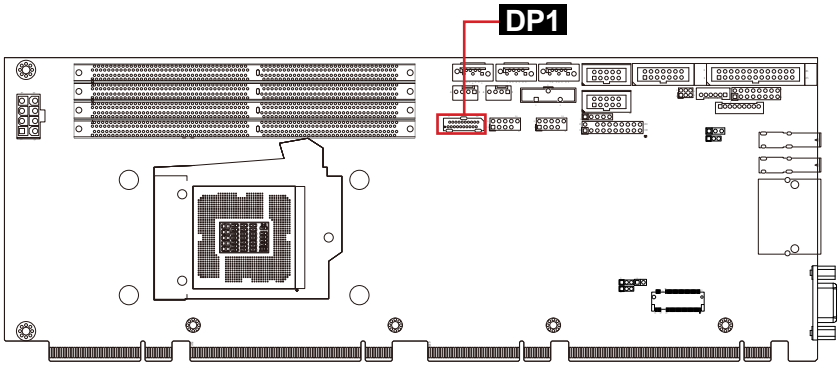




⑭DP1

Function: DisplayPort Connector
Connect the display device to the DisplayPort Connector

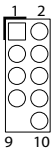
The pin assignments conform to the industry standard.

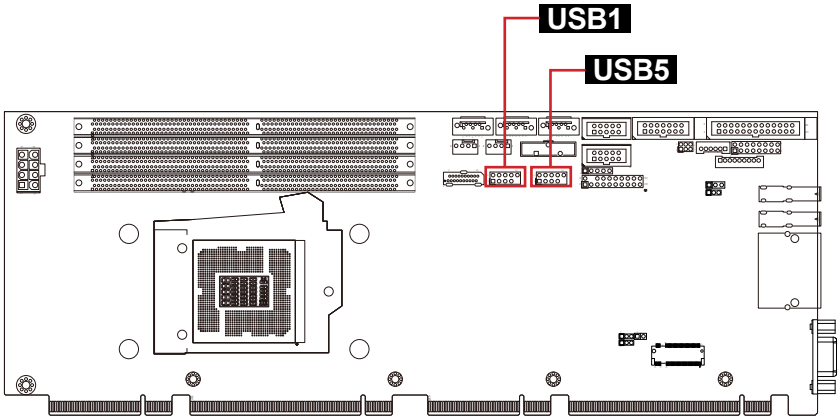


⑮⑯USB1&5

Function: USB2.0 Connector
Connector type: 2.54mm pitch 2x5 pin-headers

Pin	Desc.	Pin	Desc.
1	+V5S	2	+V5S
3	USBPN	4	USBPN
5	USBPP	6	USBPP
7	GND	8	GND
9	N/C	10	GND

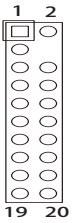


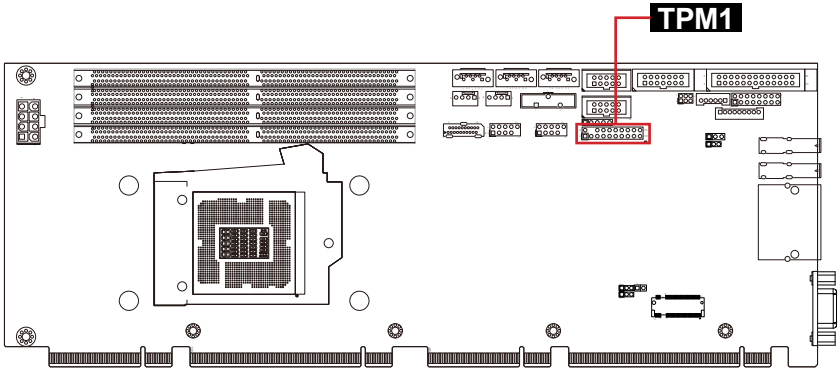


⑰TPM1

Function: TPM Connector
Connector type: 2.54mm pitch 2x10-pin headers

Pin	Desc.	Pin	Desc.
1	CLK_LPC1_24M	2	GND
3	L_FRAME#	4	N/C
5	PLT_RST	6	N/C
7	L_AD3	8	L_AD2
9	+V3.3S	10	L_AD1
11	L_AD0	12	GND
13	N/C	14	N/C
15	+V3.3A	16	SER_IRQ
17	GND	18	CLKR#
19	LPCPD#_LPC	20	N/C

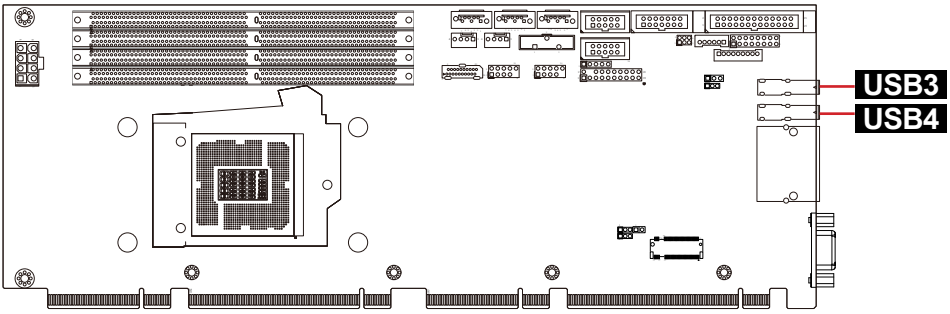




⑱⑲USB3&4

Function: USB 3.0/2.0 Connectors
Connector type: USB connectors

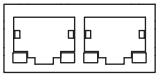
The pin assignments conform to the industry standard.

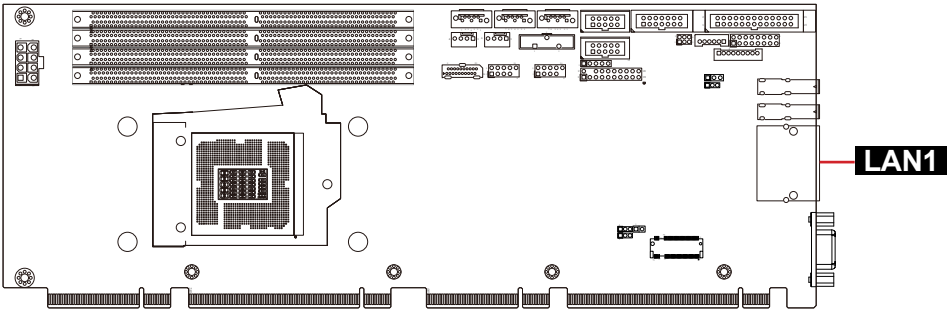


⑳LAN1

Function: GbE Connectors
Connector type: Dual RJ-45 Gbe LAN with LED indicators

The pin assignments conform to the industry standard.

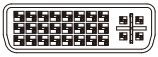




㉑DVI1/VGA1

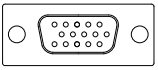
Function: DVI-I Connector (for HiCore-i89Q1)
Connector type: DVI-I connector

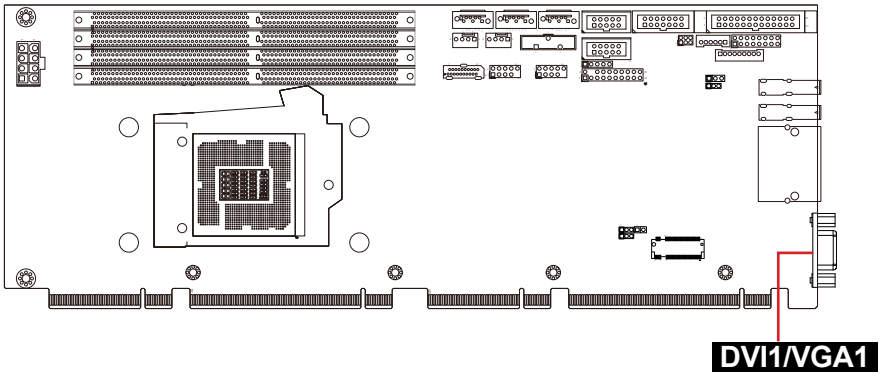
The pin assignments conform to the industry standard.



Function: VGA Connector (for HiCore-i89Q2)
Connector type: D-Sub 15-pin female connector

Pin	Desc.	Pin	Desc.
1	RED	9	5V
2	GREEN	10	GND
3	BLUE	11	N/C
4	N/C	12	D-DATA
5	GND	13	H-SYNC
6	GND	14	V-SYNC
7	GND	15	D-DCLK
8	GND		



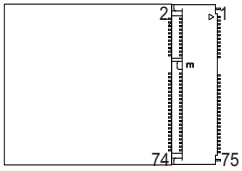


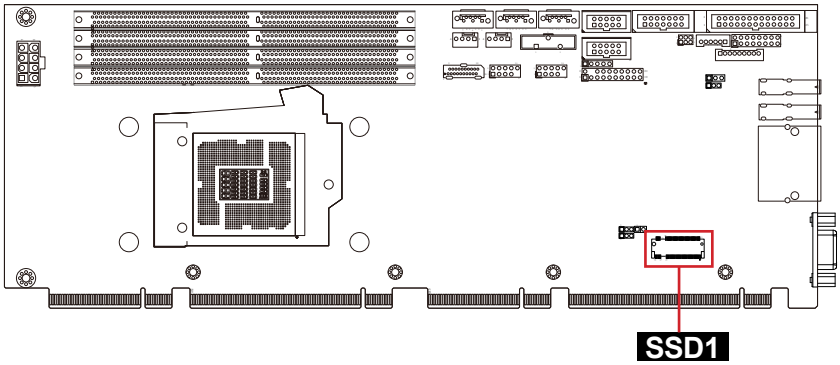
* The graphic interface depends on your model. The figure is using HiCore-i89Q1's DVI port as an example.

㉒SSD1

Function: NGFF M-Key Socket
Connector type: NGFF M-Key Socket for storage

The pin assignments conform to the industry standard.

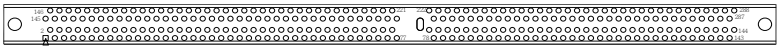


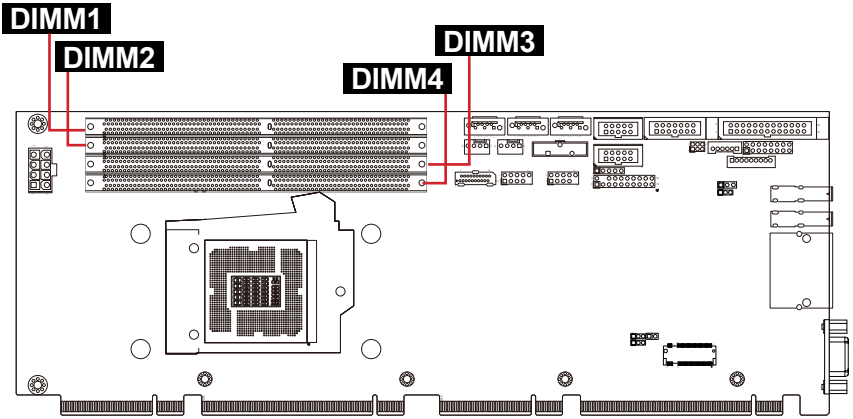


㉓㉔㉕㉖ DIMM1, 2, 3, 4

Function: DDR4 Memory Slots
Connector type: 288-pin DDR4 DIMM slots

The pin assignments conform to the industry standard.





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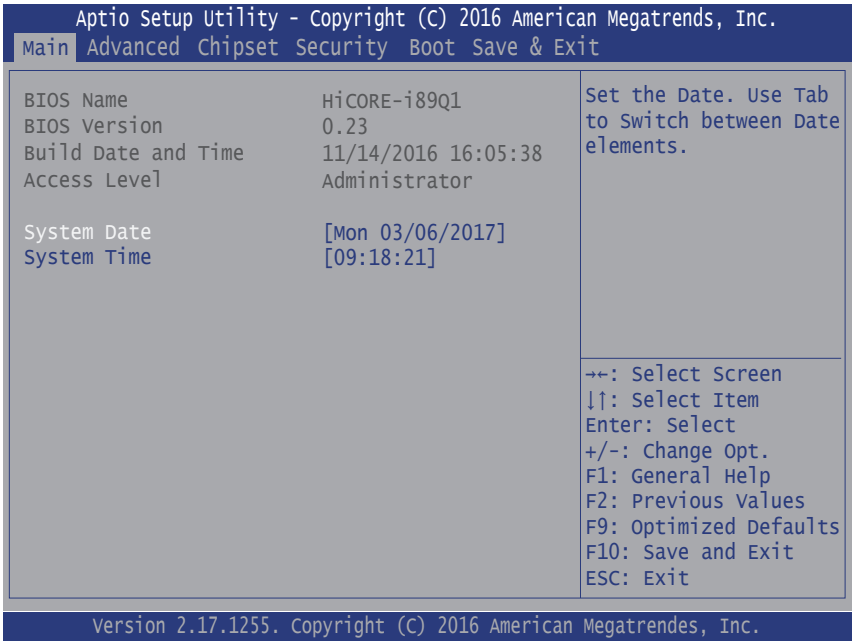
Chapter 3

BIOS

3.1 Main

The AMI BIOS provides a Setup utility program for specifying the system configurations and settings. The BIOS RAM of the system stores the Setup utility and configurations. When you turn on the computer, the AMI BIOS is immediately activated. To enter the BIOS SETUP UTILITY, press **"Delete"** once the power is turned on.

The **Main Setup** screen lists the following information:



Setting	Description
System Date	Set the system date. Use Tab to switch between Data elements. Note that the 'Day' automatically changes when you set the date. ► The date format is: **Day:** Sun to Sat **Month:** 1 to 12 **Date:** 1 to 31 **Year:** 1998 to 2099

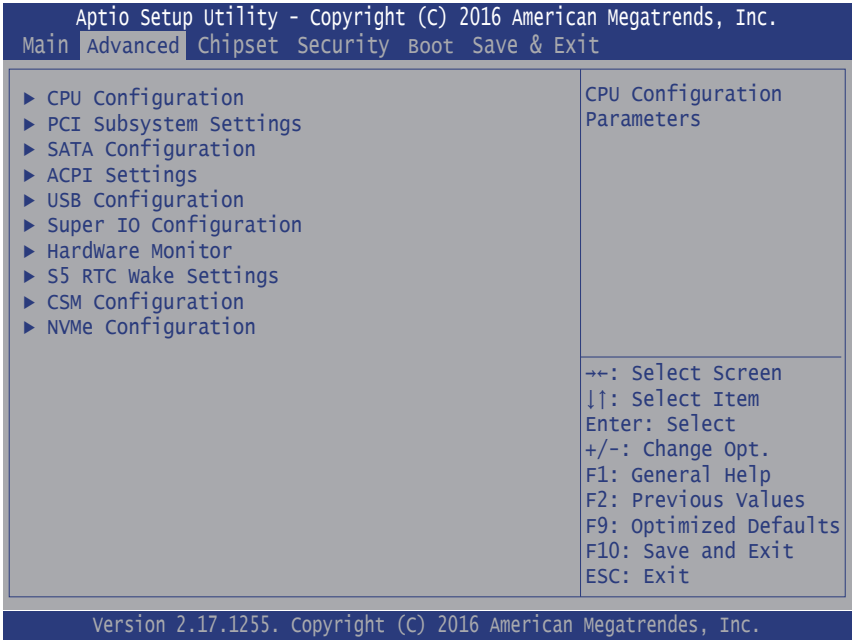
System Time	Set the system time. Use Tab to switch between Time elements. ► The time format is: **Hour:** 00 to 23 **Minute:** 00 to 59 **Second:** 00 to 59

Key Commands

BIOS Setup Utility is mainly a key-based navigation interface. Please refer to the following key command instructions for navigation process.

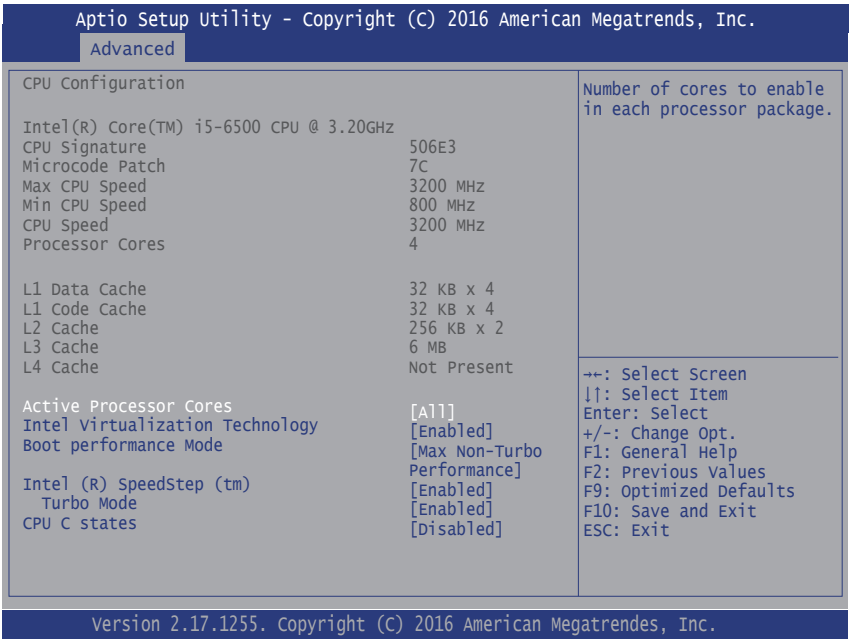
Keystroke	Function
◄ ►	Move to highlight a particular configuration screen from the top menu bar / Move to highlight items on the screen
▼ ▲	Move to highlight previous/next item
Enter	Select and access a setup item/field
Esc	On the Main Menu – Quit the setup and not save changes into CMOS (a message screen will display and ask you to select “OK” or “Cancel” for exiting and discarding changes. Use “←” and “→” to select and press “Enter” to confirm) On the Sub Menu – Exit current page and return to main menu
Page Up / +	Increase the numeric value on a selected setup item / make change
Page Down / -	Decrease the numeric value on a selected setup item / make change
F1	Activate “General Help” screen
F10	Save the changes that have been made in the setup and exit. (a message screen will display and ask you to select “OK” or “Cancel” for exiting and saving changes. Use “←” and “→” to select and press “Enter” to confirm)

3.2 Advanced



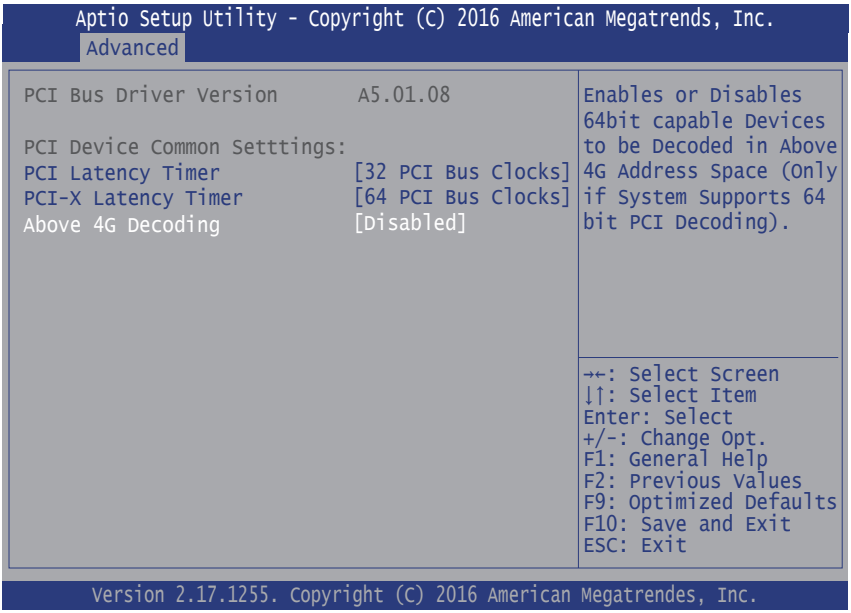
Setting	Description
CPU Configuration	See section 3.2.1 CPU Configuration on page 41
PCI Subsystem Settings	See section 3.2.2 PCI Subsystem Settings on page 42
SATA Configuration	See section 3.2.3 SATA Configuration on page 43
ACPI Settings	See section 3.2.4 ACPI Settings on page 44
USB Configuration	See section 3.2.5 USB Configuration on page 45
Super IO Configuration	See section 3.2.6 Super IO Configuration on page 47
Hardware Monitor	See section 3.2.7 Hardware Monitor on page 49
S5 RTC Wake Settings	See section 3.2.8 S5 RTC Wake Settings on page 50
CSM Configuration	See section 3.2.9 CSM Configuration on page 51
NVMe Configuration	See section 3.2.10 NVMe Configuration on page 52

3.2.1 CPU Configuration



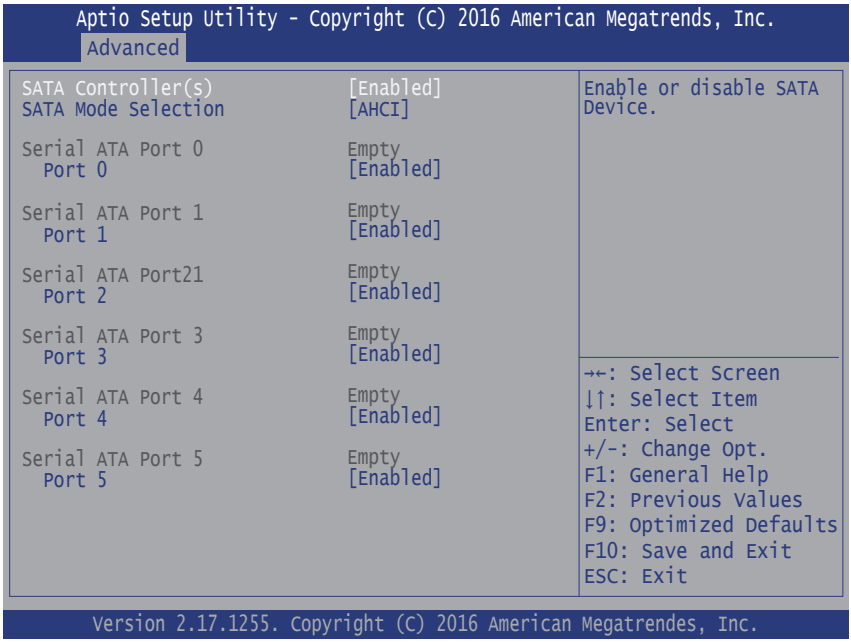
Setting	Description
Active Processor Cores	Number of cores to enable in each processor package. ► Options: **All** (default), **1**, **2** and **3.**
Intel Virtualization Technology	When enabled, a VMM can utilize the additional hardware capabilities provided by Vanderpool Technology ► Options: **Enabled** (default) or **Disabled**
Boot performance Mode	Set the performance state that the BIOS will set before the OS handoff. ► Options: **Max Battery, Max Non-Turbo Performance** (default) and **Turbo Performance**.
Intel (R) Speed Step (tm)	**Enable** (default)/**Disable** Intel SpeedStep
Turbo Mode	Only available when Intel Speed Step is **Enabled**. **Enable** (default)/**Disable** Turbo Mode
CPU C States	**Enable** /**Disable** (default) CPU C States

3.2.2 PCI Subsystem Settings



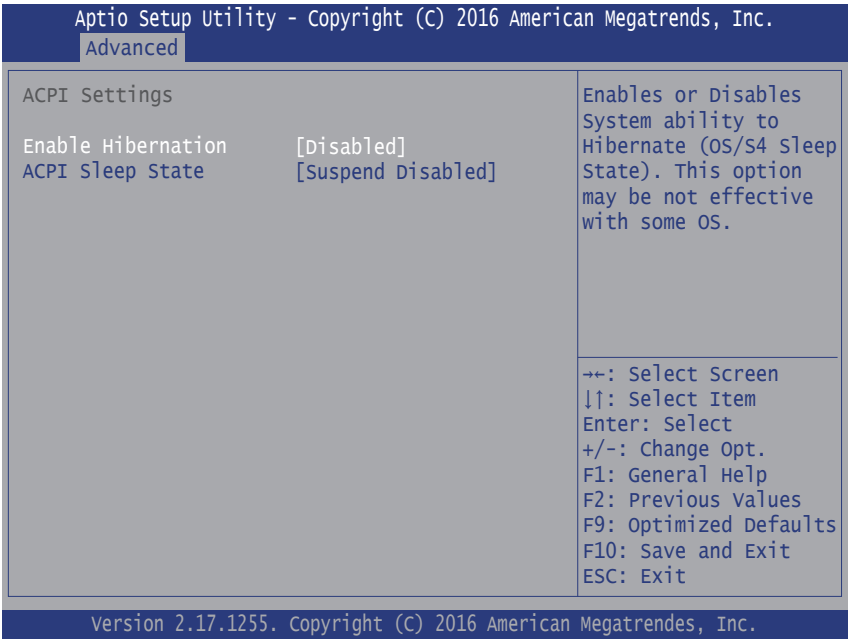
Setting	Description
PCI Latency Timer	Value to be programmed into PCI Latency Timer Register. ► **32** (default), **64**, **96**, **128**, **160**, **192**, **224** and **248 PCI Bus Clocks**.
PCI-X Latency Timer	Value to be programmed into PCI-X Latency Timer Register. ► **32**, **64** (default), **96**, **128**, **160**, **192**, **224** and **248 PCI Bus Clocks**.
Above 4G Decoding	**Enable**/**Disable** (default) 64bit capable Devices to be Decoded in Above 4G Address Space (Only if System Supports 64 bit PCI Decoding).

3.2.3 SATA Configuration



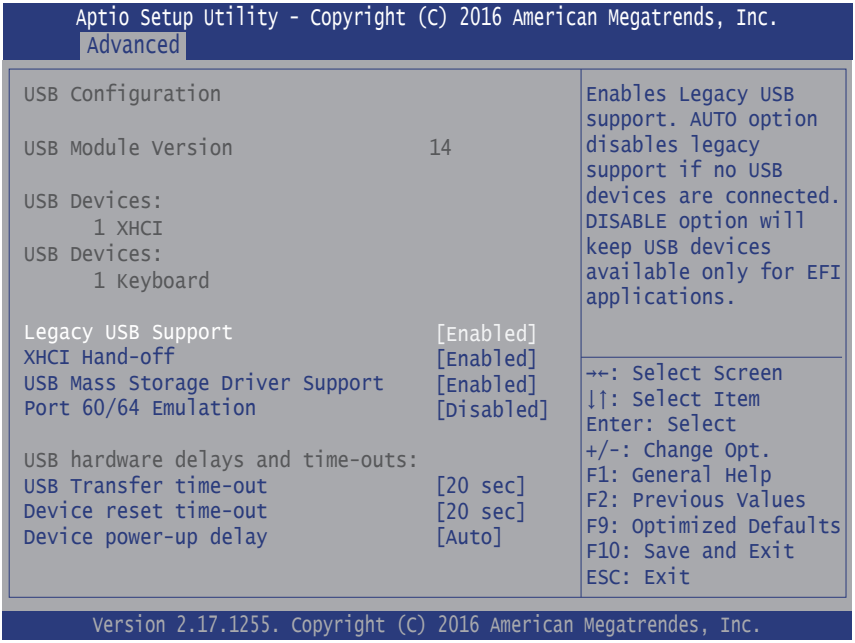
Setting	Description
SATA Controller(s)	**Enable** (default) or **disable** SATA Device.
SATA Mode Selection	Determines how SATA controller(s) operate. ► Options: **AHCI** (default) and **RAID**
Port 0/1/2/3/4/5	**Enable** (default) or **disable** SATA Port.

3.2.4 ACPI Settings



Setting	Description
Enable Hibernation	**Enable** or **Disable** (default) System ability to Hibernate (OS/S4 Sleep State). This option may be not effective with some OS.
ACPI Sleep State	Select the highest ACPI sleep state the system will enter when the SUSPEND button is pressed. ► Options: **Suspend Disabled** (default) and **S3 (Suspend to RAM)** .

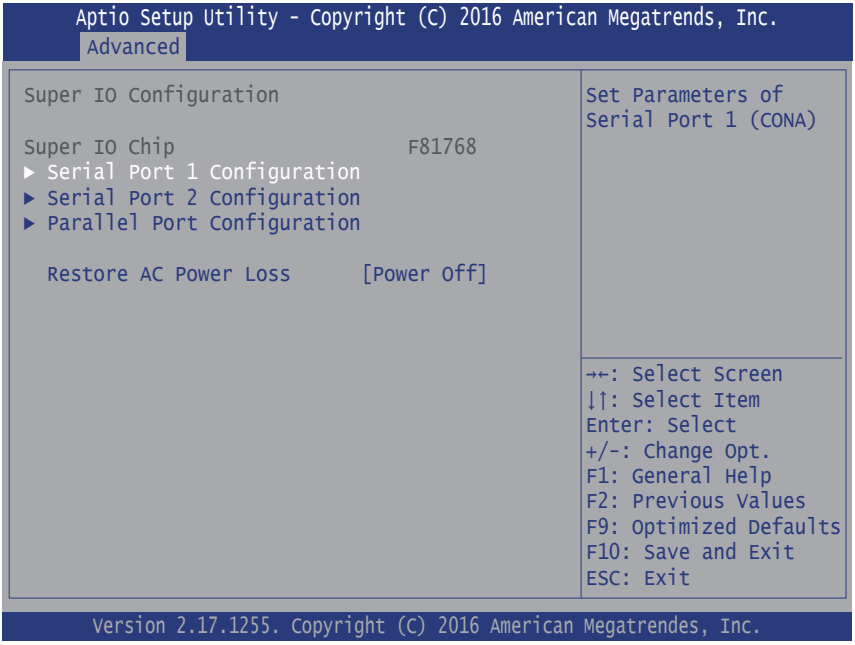
3.2.5 USB Configuration



Setting	Description
Legacy USB Support	Sets legacy USB support. ► Options: **Enabled** (default), **Disabled** and **Auto**. **AUTO** option disables legacy support if no USB devices are connected. **Disable** option will keep USB devices available only for EFI applications.
XHCI Hand-off	**Enable** (default) or **Disable** XHCI Hand-off This is a workaround for OSes without XHCI hand-off support. The XHCI ownership change should be claimed by XHCI driver.
USB Mass Storage Driver Support	**Enable** (default) or **Disable** USB Mass Storage Driver Support.

USB hardware delay and time-out	
USB Transfer time-out	Use this item to set the time-out value for control, bulk, and interrupt transfers. ▸ Options available are: **1 sec, 5 sec, 10 sec, 20 sec** (default)
Device reset time-out	Use this item to set USB mass storage device start unit command time-out. ▸ Options available are: **10 sec, 20 sec** (default)**, 30 sec, 40 sec**
Device power-up delay	Use this item to set maximum time the device will take before it properly reports itself to the host controller. ▸ Options available are: **Auto** (Default): 'Auto' uses default value: for a root port it is 100 ms, for a hub port the delay is taken from hub descriptor. **Manual**: Select **Manual** you can set value for the following sub-item: '**Device Power-up delay in seconds**', the delay range in from 1 to 40 seconds, in one second increments.

3.2.6 Super IO Configuration



Setting	Description
Serial Port 1/2 & Parallel Port Configuration	See next page.
Restore AC Power Loss	Specify what state to go to when power is re-applied after a power failure. ► Options: **Last State**, **Power On** and **Power Off** (default)

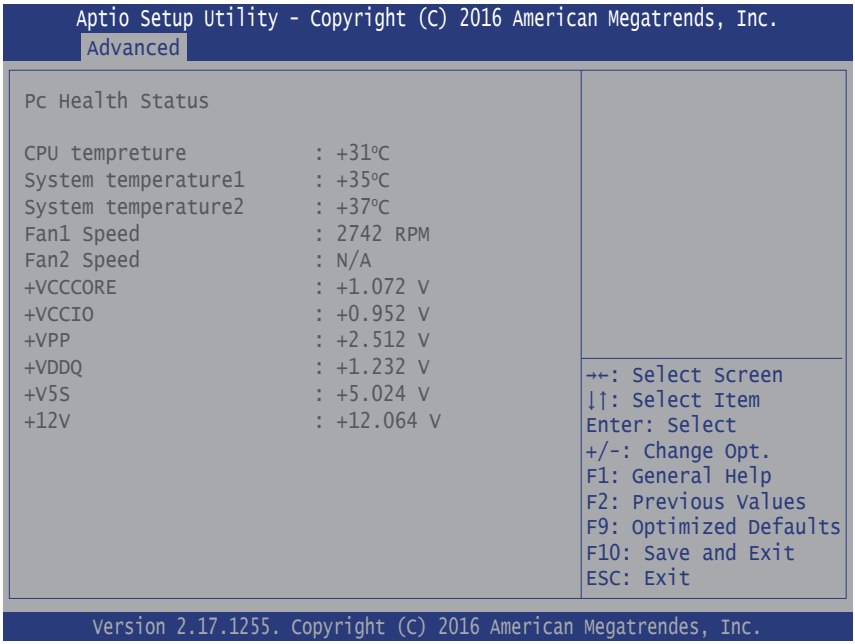
Serial Port 1/2 Configuration

Setting	Description
Serial Port	**Enable** (default) or **Disable** Serial Port (COM).
Change Settings	Select an optimal setting for Super IO device. ► Options for Serial Port 1: **Auto**; **IO=3F8h; IRQ=4** (default) ; **IO=3F8h; IRQ=3, 4, 5, 6, 7, 9, 10, 11, 12**; **IO=2F8h; IRQ=3, 4, 5, 6, 7, 9, 10, 11, 12**; **IO=3E8h; IRQ=3, 4, 5, 6, 7, 9, 10, 11, 12**; **IO=2E8h; IRQ=3, 4, 5, 6, 7, 9, 10, 11, 12**; ► Options for Serial Port 2: **Auto** **IO=2F8h; IRQ=3** (default) **IO=3F8h; IRQ=3, 4, 5, 6, 7, 9, 10, 11, 12**; **IO=2F8h; IRQ=3, 4, 5, 6, 7, 9, 10, 11, 12**; **IO=3E8h; IRQ=3, 4, 5, 6, 7, 9, 10, 11, 12**; **IO=2E8h; IRQ=3, 4, 5, 6, 7, 9, 10, 11, 12**;
RS-485 AutoFlow	This option is only available for Serial Port 2. **Enable** or **Disable** (default) RS-485 AutoFlow.

Parallel Port Configuration

Setting	Description
Parallel Port	**Enable** (default) or **Disable** Parallel Port (LPT/LPTE).
Change Settings	Select an optimal setting for Super IO device. ► Options: **Auto** **IO=378h; IRQ=7** (default) **IO=378h; IRQ=5, 6, 7, 9, 10, 11, 12** **IO=278h; IRQ=5, 6, 7, 9, 10, 11, 12** **IO=3BCh; IRQ=5, 6, 7, 9, 10, 11, 12**
Device Mode (only for Parallel Port Configuration)	Change the Printer Port mode. ► Options: **STD Printer Mode** (default) **SPP Mode** **EPP-1.9 and SPP Mode** **EPP-1.7 and SPP Mode** **ECP Mode** **ECP and EPP 1.9 Mode** **ECP and EPP 1.7 Mode**.

3.2.7 Hardware Monitor

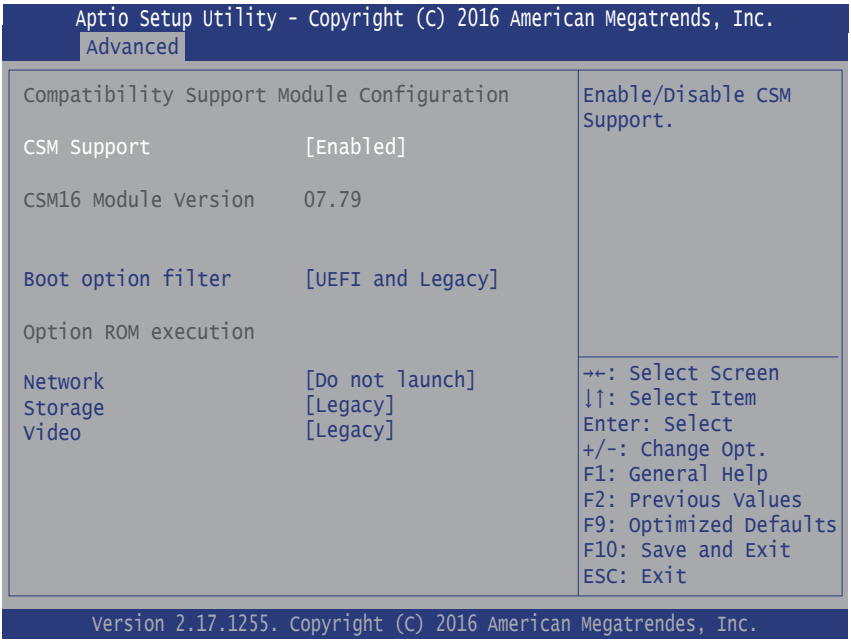


Access this submenu to monitor the hardware status.

3.2.8 S5 RTC Wake Settings

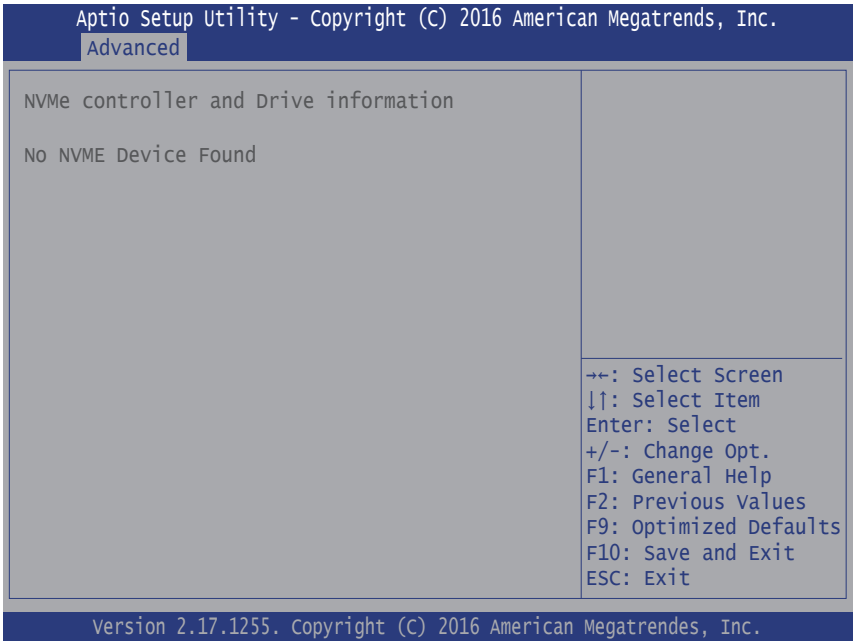
Setting	Description
Wake System from S5	**Enable** or **Disable** (default) system wake on alarm event. ► Options available are: **Disabled** (default): **Fixed Time:** System will wake on the hr::min::sec specifiedc. **DynamicTime:** If selected, you need to set **Wake up minute increase** from 1 - 5. System will wake on the current time + increase minute(s).

3.2.9 CSM Configuration



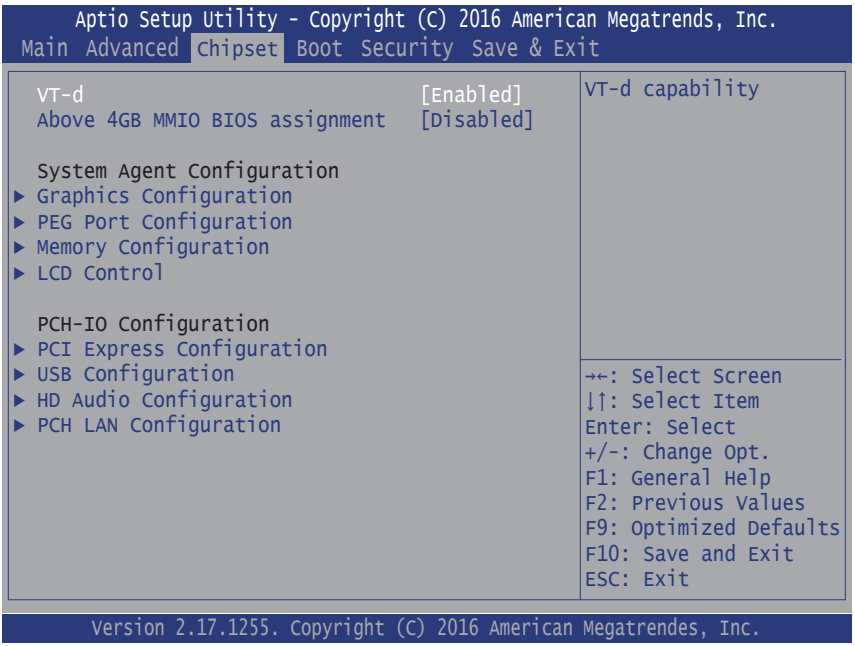
Setting	Description
CSM Support	**Enable** (default) or **Disable** CSM Support.
Boot option filter	Control the Legacy/UEFI ROMs priority. ► Options: **UEFI and Legacy** (default), **Legacy only**, **UEFI only**
Network	Control the execution of UEFI and Legacy PXE OpROM ► Options: **Do not launch** (default) and **Legacy**
Storage	Control the execution of UEFI and Legacy Storage OpROM ► Options: **Do not launch** and **Legacy** (default)
Video	Control the execution of UEFI and Legacy Video OpROM ► Options: **UEFI** and **Legacy** (default)

3.2.10 NVMe Configuration



Access this submenu to view the NVME device information.

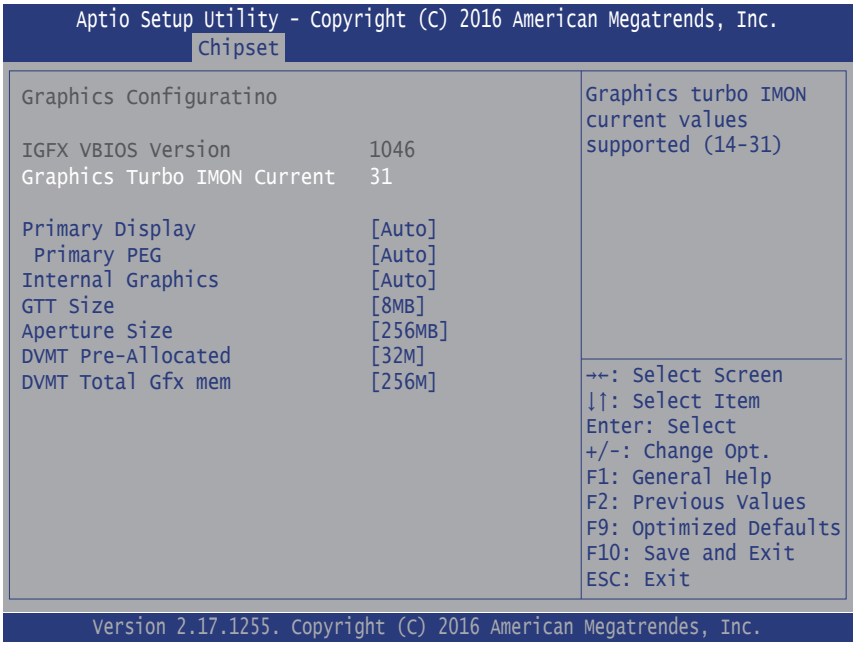
3.3 Chipset



Setting	Description
VT-d	**Enable** (default) or **Disable** VT-d function
Above 4GB MMIO BIOS assignment	**Enable** or **Disable** (default) Above 4GB MMIO BIOS assignment
System Agent (SA) Configuration	
Graphics Configuration	See section 3.3.1 Graphics Configuration on page 55
PEG Port Configuration	See section 3.3.2 PEG Port Configuration on page 57
Memory Configuration	See section 3.3.3 Memory Configuration on page 58
LCD Control	See section 3.3.4 LCD Control on page 59
PCH-IO Configuration	

PCI Express Configuration	See section 3.3.5 PCI Express Configuration on page 60
USB Configuration	See section 3.3.6 USB Configuration on page 61
HD Audio Configuration	Control Detection of the HD-Audio device. ► Options available are: **Disabled**: HDA will be unconditionally disabled **Enabled** (default) : HDA will be unconditionally Enabled **Auto** = HDA will be enabled if present, disabled otherwise.
PCH LAN Controller	Enables/Disables onboard NIC. ► Options: **Enabled** (default) and **Disabled** If enabled, “Wake on LAN” option will be available to **Enable** (default) / **Disable** integrated LAN to wake the system. (the Wake On LAN cannot be disabled if ME is on at Sx state.)

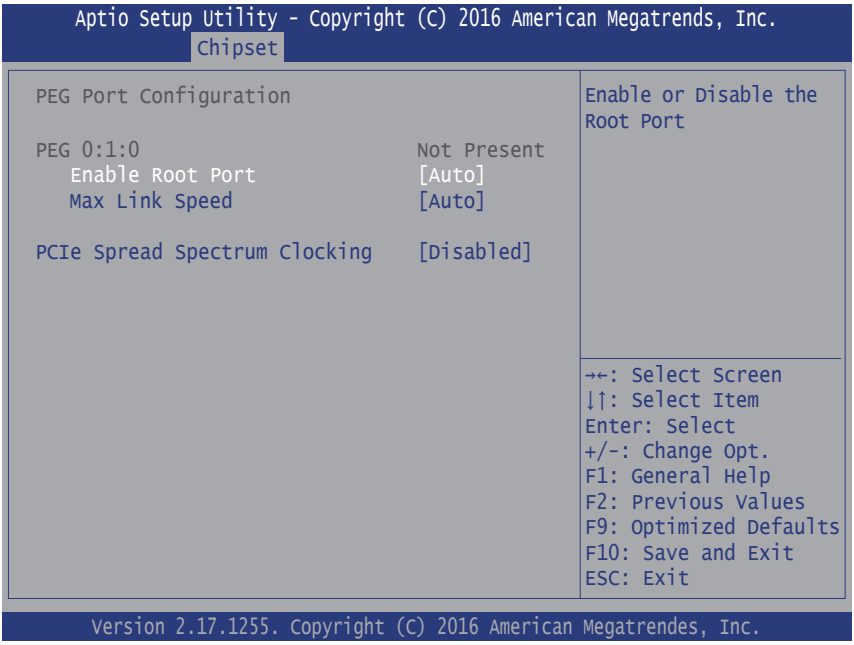
3.3.1 Graphics Configuration



Setting	Description
Graphics Turbo IMON Current	Sets the graphics turbo IMON current values. ► Options available are **14** to **31** (default).
Primary Display	Select which of IGFX/PEG/PCI Graphics device should be Primary Display or select SG for Switchabel Gfx. ► Options available are **Auto** (default), IGFX and PEG.
Primary PEG	Set the Primary PEG device. ► Options: **Auto** (default)**, PEG11,** and **PEG12**.
Internal Graphics	Keep IGD enabled based on the setup options. ► Options: **Auto** (default)**, Disabled** and **Enabled**.

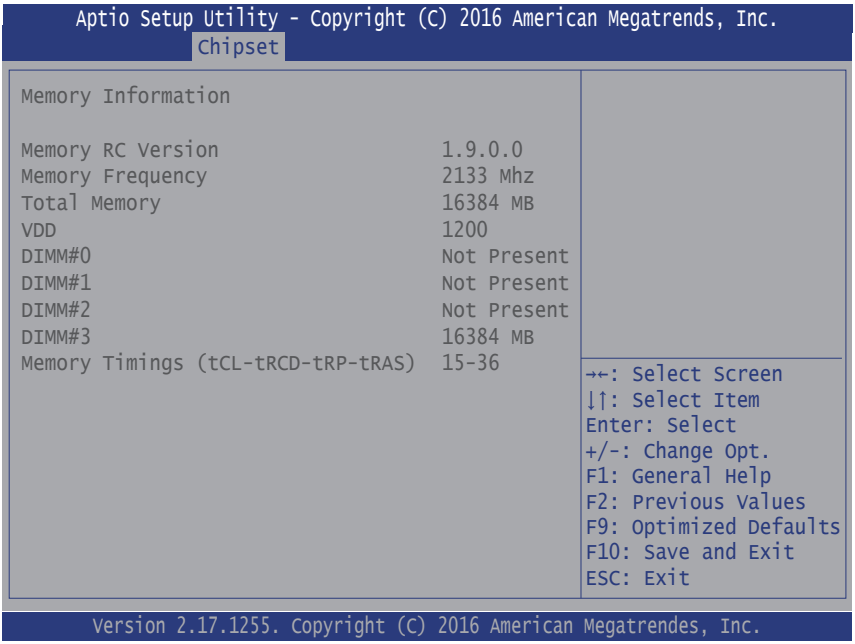
GTT Size	Select the GTT Size. ► Options: **4MB, 2MB** and **8MB** (default)**.**
Apeture Size	Select the Apeture Size. Note that above 4GB MMIO BIOS assignment is automatically enabled when selecting 2048MB aperture. To use this feature, please disable CSM support. ► Options: **128MB**, **256MB** (default)**, 512MB**, **1024MB**, **2048MB** and **4096MB**.
DVMT Pre-Allocated	Select the DVMT 5.0 Pre-allocated (Fixed) Graphic Memory size used by the Internal Graphic Device. ► Options: **32M** is the default.
DVMT total Gfx Mem	Select the DVMT 5.0 Total Graphic Memory size used by the Internal Graphic Device. ► Options: **128MB, 256MB** (default) and **Max.**

3.3.2 PEG Port Configuration



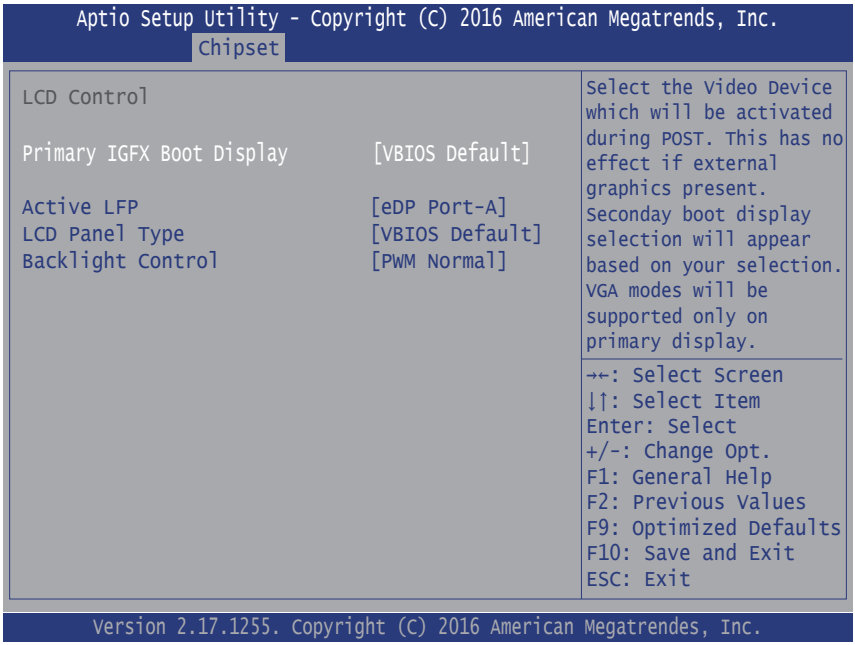
Setting	Description
Enable Root Port	Configures the Root Port. ► Options: **Auto** (default), **Enabled** and **Disabled**.
Max Link Speed	Configures PEG 0:1:0 Max Speed. ► Options: **Auto** (default), **Gen1**, **Gen2** and **Gen3**.
PCIe Spread Spectrum Clocking	Allows to **Enable** / **Disable** (default) Spread Spectrum Clocking for compliance testing.

3.3.3 Memory Configuration



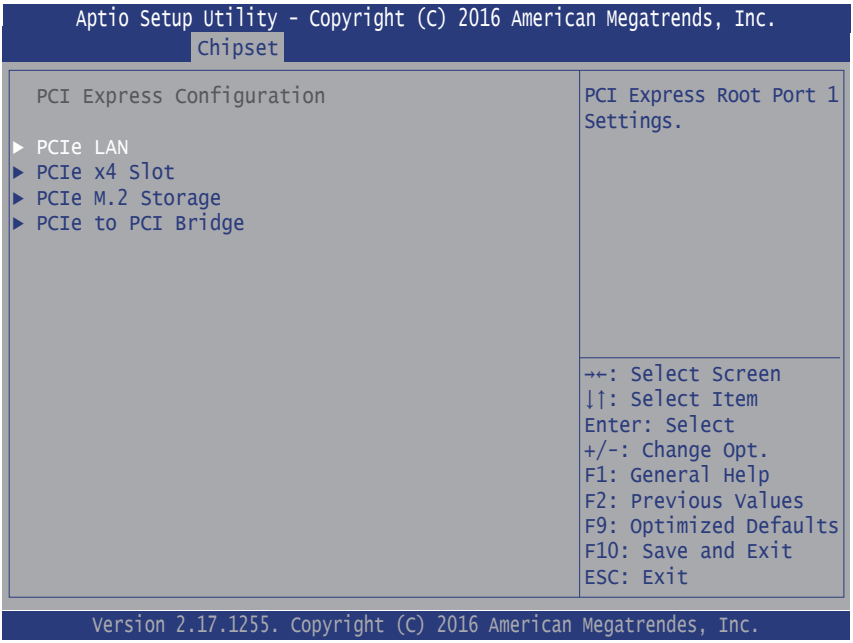
Access this submenu to view the memory configuration.

3.3.4 LCD Control



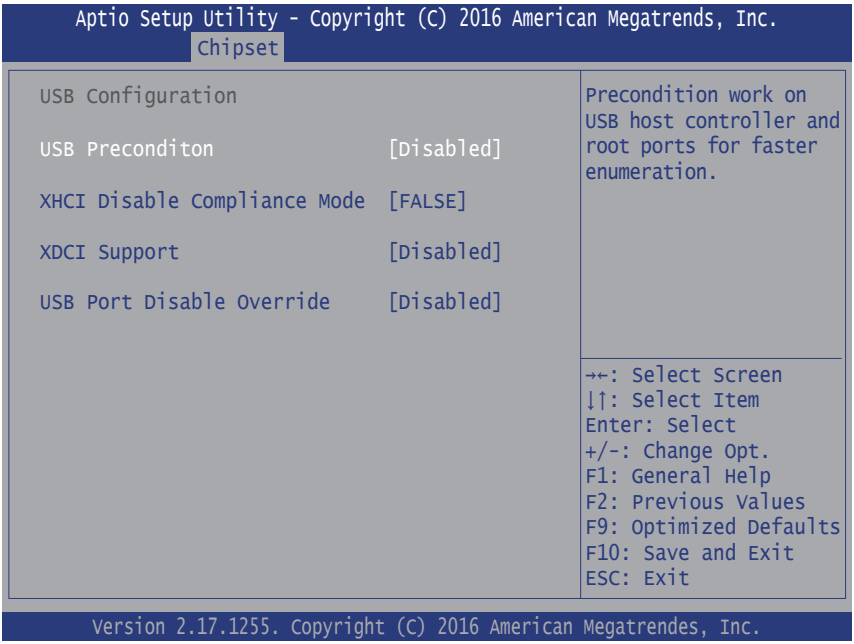
Setting	Description
Primary IGFX Boot Display	Select the Video Device which will be activated during POST. This has no effect if external graphics present. Secondary boot display selection will appear based on your selection. VGA modes will be supported only on primary display. ► Options: **VBIOS Default** (default), **DVI**, **DP** and **EFP3**.
Active LFP	Configuring LFP usage ► Options: **No LVDS** and **eDP Port-A** (default)
LCP Panel Type	Select LCD panel used by Internal Graphics Device by selecting the appropriate setup item. The default is **VBIOS Default**.
Backlight Control	Configuring Backlight control setting. ► Options: **PWM Inverted** and **PWM Normal** (default)

3.3.5 PCI Express Configuration



Setting		Description
PCIe LAN, PCIe x4 Slot, PCIe M.2 Storage	Port	**Enable** (default) or **Disable** the PCIe Express Root Port.
	ASPM Support	Disable or set the ASPM level. Force L0s will force all inks to L0s state. “Auto” will allow BIOS to auto configure.”Disable” will disable ASPM. ► Options: **Disabled** (default), **L0s**, **L1**, **L0sL1** and **Auto**.
	PCIe Speed	Select PCI Express port speed. ► Options: **Auto** (default), **Gen1**, **Gen2** and **Gen3**
PCIe to PCI Bridge		**Enable** or **Disable** (default) the PCIe Express Root Port.

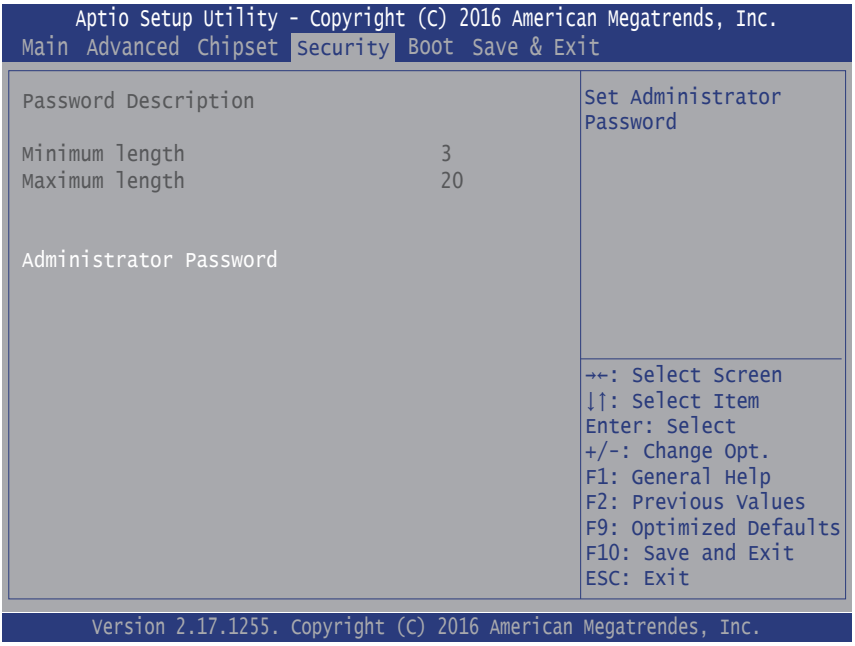
3.3.6 USB Configuration



Setting	Description
USB Precondition	Precondition work on USB host controller and root ports for faster enumeration. ► Options: **Enable**/**Disable** (default).
XHCI Disable Compliance Mode	Options to disable Compliance Mode. Default is FALSE to not disable Compliance Mode. Set TRUE to disable Compliance Mode. ► Options: **False** (default)/**True**.
xDCI Support	**Enable** or **Disable** (default) xDCI (USB OTG Device.
USB Port Disable Override	Selectively enable/disable the corresponding USB port from reporting a Device Connection to the controller. ► Options: **Disabled** (default) / **Select Per-Pin**.

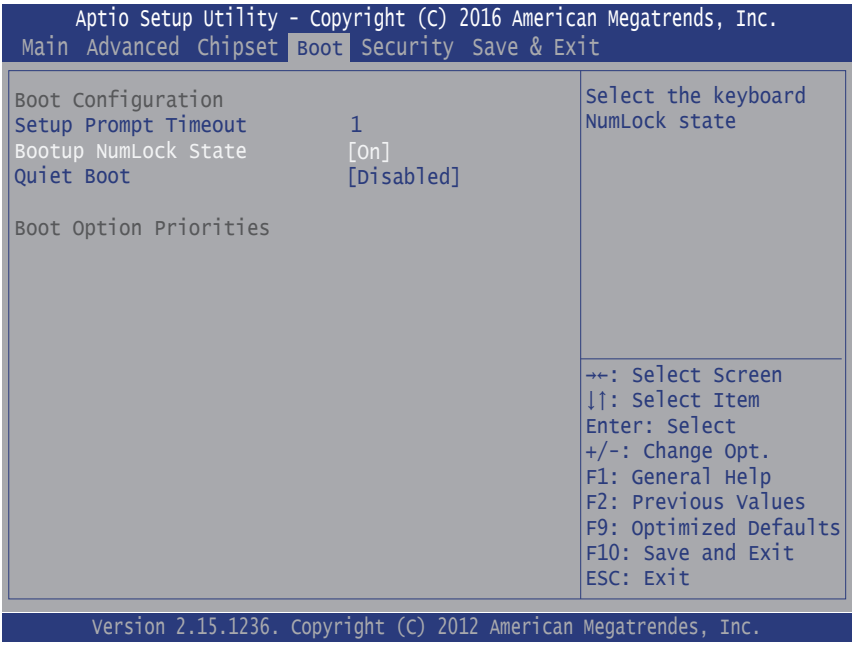
3.4 Security

The **Security** menu sets up the administrator password.



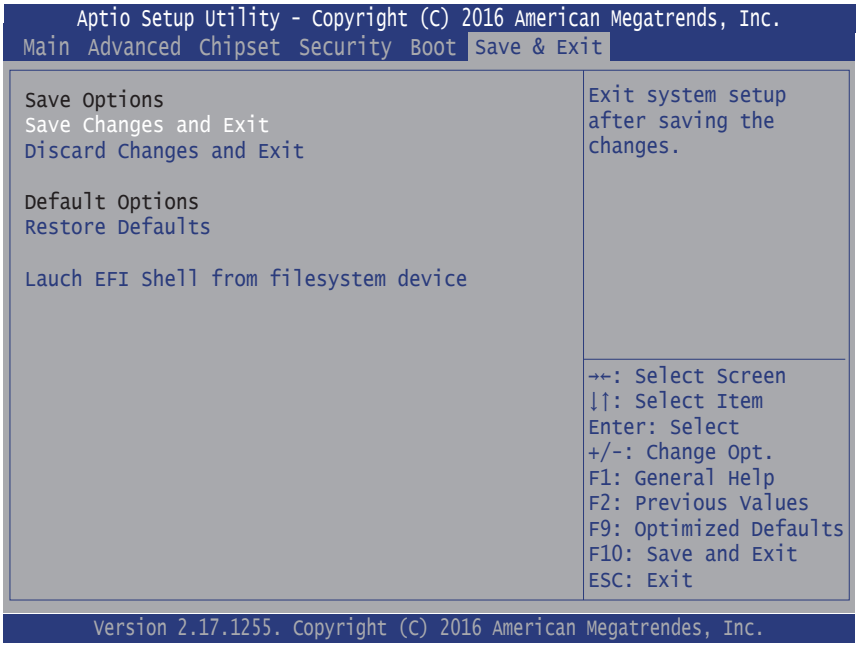
Setting	Description
Administrator Password	To set up an administrator password: 1. Select **Administrator Password**. The screen then pops up an **Create New Password** dialog. 2. Enter your desired password that is no less than 3 characters and no more than 20 characters. 3. Hit [Enter] key to submit.

3.5 Boot



Setting	Description
Setup Prompt Timeout	Number of seconds to wati for setup activation key. 65535 (0XFFFF) means indefinite waiting.
Boot NumLock State	Select the keyboard NumLock state. ► Options: **On** (default) and **Off**.
Quiet Boot	**Enable** or **Disable** (default) Quiet Boot option.

3.6 Save & Exit



Setting	Description
Save Changes and Exit	Exit system setup after saving the changes. ► Enter the item and then a dialog box pops up: **Save configuration and exit? (Yes/ No)**
Discard Changes and Exit	Exit system setup without saving the changes. ► Enter the item and then a dialog box pops up: **Quit without saving? (Yes/ No)**
Restore Defaults	Restore/Load Default values for all the setup options. ► Enter the item and then a dialog box pops up: **Load Optimized Defaults? (Yes/ No)**
Launch EFI Shell from filesystem device	Attempts to launch EFI shell application (Shell.efi) from one of the available filesystem devices.

Appendix

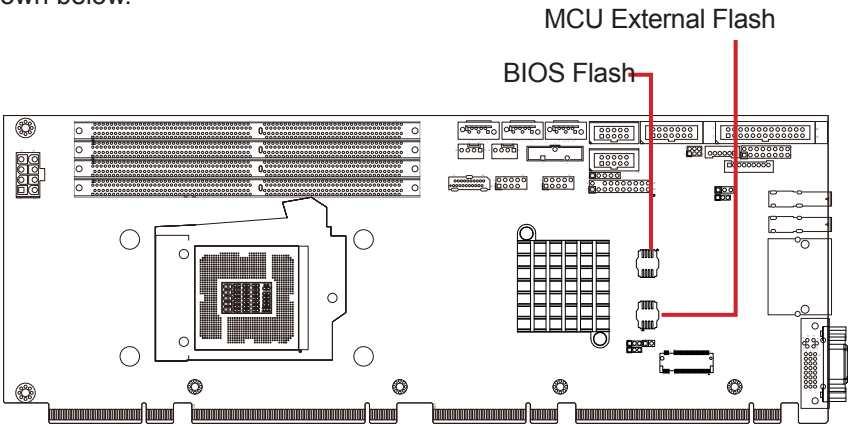
Appendix A. Anti-Crash Technology for BIOS Recovering

The motherboard supports Anti-Crash Technology (ACT) for automatical system BIOS recovering. This section describes the recovery and update process.

Caution: DO NOT disconnect the AC power supply during the Auto Recovery and BIOS update process.

A.1 Auto Recovery

The motherboard comes with two BIOS ROMs mounted onto the board as shown below.



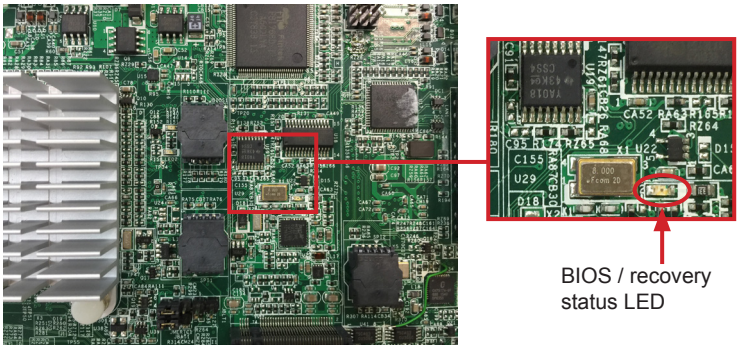
- BIOS Flash: Master ROM for BIOS
- MCU External Flash: Slave ROM for backup BIOS

In case the motherboard fails to boot, it will run BIOS self diagnostics to verify the BIOS status on the master ROM. If problem is detected on the BIOS, then the recovery process will automatically start to load the backup BIOS from the slave ROM. The whole process will take about 2~3 minutes where a BIOS recovery status LED will show the recovery status as described below:

- The LED blinks fast to indicate erasing data from the master ROM.
- The LED blinks slowly to indicate the MCU is writing system backup BIOS from the slave ROM to the master one.

- The LED turns off to indicate the process is finished and the motherboard will automatically boot to your system.

If you cannot see the LED status, just **wait for about 3 minutes** for the motherboard to complete the recovery and then reboot to your system.



A.2 BIOS Update using ACT Utility

When a new version of BIOS is available and you want to update the BIOS, you need to update the BIOS in the master ROM as well as the slave ROM to the same version; otherwise the master BIOS will load a different version upon BIOS recovery.

ARBOR's proprietary ACT Utility is designed to update the BIOS in the master ROM as well as the slave ROM at the same time. The ACT Utility is a DOS-based program:

```
C:\I89Q1>dir /w
Volume in drive C is DOS USB
Volume Serial Number is D0A5-AA5A
Directory of C:\I89Q1

[.]           [..]  89Q1.BAT       BACKUP.EXE      ERROR.LOG
FPARTS.TXT    FPT11.EXE            I89Q1.023       UPDATE.EXE
      7 file(s)    18,475,016 bytes
      2 dir(s)      2,590.02 MB free

C:\I89Q1>89q1
```

After running the program on command prompt, the utility performs these tasks:

1. Provides a specific protection to the BIOS. This ensures the BIOS will not become corrupted if power failure occurs while the BIOS update is in progress.
2. Update the BIOS in master ROM to the new version.

```
[.]           [..]  89Q1.BAT       BACKUP.EXE      ERROR.LOG
FPARTS.TXT    FPT11.EXE            I89Q1.023       UPDATE.EXE
      7 file(s)    18,475,016 bytes
      2 dir(s)      2,590.02 MB free

C:\I89Q1>89q1
C:\I89Q1>update.exe
C:\I89Q1>fpt11.exe - SAVEMAC  -F i89Q1.023

Intel (R) Flash Programming Tool. Version:   11.0.0.1202
Copyright (c) 2007 - 2015, Intel Corporation. All rights reservation

Reading HSFSTS register...Flash Descriptor: Valid

o--- Flash Devices Found ---
oW25Q128BVoID:0xEF4048oSize: 16384KB (131072Kb)

PDR Region does not exists.
```

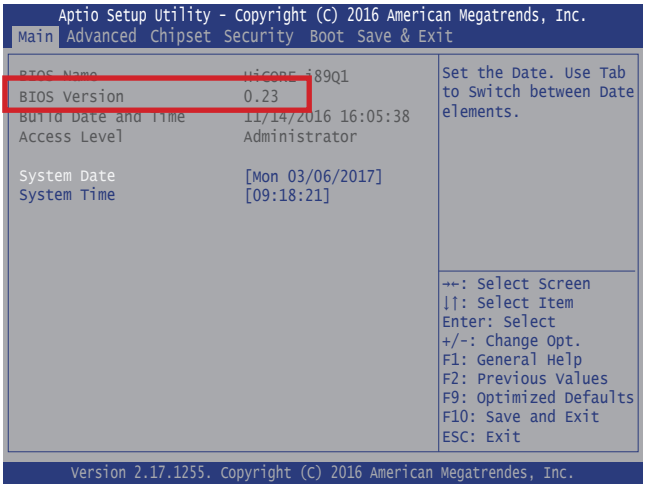
```
PDR Region does not exists.
- Reading Flash [0x016B000]     - 100 percent complete.
- Programming Flash [0x016B000]   88KB of  88KB - 100 percent complete.
- Erasing Flash Block [0x274000] - 100 percent complete.
- Programming Flash [0x274000]   - 12KB of 12KB - 100 percent complete.
- Erasing Flash Block [0xA0A000] - 100 percent complete.
- Programming Flash [0xA0A000]   - 40KB of 40KB - 100 percent complete.
- Erasing Flash Block [0x0A2000] - 100 percent complete.
- Programming Flash [0x0A2000]   - 4KB of  4KB  - 100 percent complete.
- Erasing Flash Block [0xA51000] - 100 percent complete.
- Programming Flash [0xA51000]   - 4KB of 4KB  - 100 percent complete.
- Erasing Flash Block [0xA59000] - 100 percent complete.
- Programming Flash [0xA59000]   - 8KB of 8KB  - 100 percent complete.
- Erasing Flash Block [0x882000] - 62 percent complete.
```

3. Backup the new version of BIOS to the slave ROM. During this stage:
   - The system will shut down and the screen goes black.
   - The BIOS recovery status LED blinks fast to indicate erasing data from the slave ROM.

- The BIOS recovery status LED blinks slowly to indicate the MCU is writing system BIOS from the mater ROM to the slave one.

4. Once the programming procedure is done, the computer soon reboots to verify if both the master/slave BIOS functions properly. If yes, then the computer will boot to your system.

After using the ACT Utility to perform the BIOS update, user can verify the BIOS version by accessing the BIOS:



A.3 How to Get ACT Utility

ARBOR's ACT Utility is provided upon request. Please contact your local ARBOR sales office or sales representativ for more information.

Appendix B. Watchdog Timer (WDT) Setting

WDT is widely used for industrial application to monitor CPU activities. The application software depends on its requirement to trigger WDT with adequate timer setting. Before WDT timeout, the functional normal system will reload the WDT. The WDT never time-out for a normal system. The WDT will not be reloaded by an abnormal system, then WDT will time-out and auto-reset the system to avoid abnormal operation.

This computer supports 255 levels watchdog timer by software programming I/O ports.

Below is an program example to disable and load WDT.

Sample Codes:

```
/*-----   Include Header Area -----*/
#include "math.h"
#include "stdio.h"
#include "dos.h"

unsigned char sioIndex  = 0x2E;                                  /* or index = 0x4E */
unsigned char sioData   = 0x2F;                                  /* or data  = 0x4F */

/*-----   routing, sub-routing -----*/
void main()
{
          outportb(sioIndex, 0x87);                              /* Enable Super I/O */
          outportb(sioIndex, 0x87);

          outportb(sioIndex, 0x07);                              /* Select logic device -
WDT */
          outportb(sioData,  0x07);

          outportb(sioIndex, 0x30);                              /* Enable WDT */
          outportb(sioData,  0x01);

          outportb(sioIndex, 0xF0);                              /* Enable WDTRST# Output
*/
          outportb(sioData,  0x80);

          outportb(sioIndex, 0xF6);                              /* Set WDT Timeout value
*/
          outportb(sioData,  0x05);

          outportb(sioIndex, 0xF5);                              /* Set Configure and En-
able WDT timer, Start countdown */
          outportb(sioData,  0x32);

          outportb(sioIndex, 0xAA);                              /* SIO - Disable */
}
```

Appendix C. Digital I/O Setting

Digital I/O can read from or write to a line or an entire digital port, which is a collection of lines. This mechanism helps users achieve various applications such as industrial automation, customized circuit, and laboratory testing. Take the source code below that is written in C for the digital I/O application example.

Sample Codes:

```
/*-----   Include Header Area -----*/
#include "math.h"
#include "stdio.h"
#include "dos.h"

#define    sioIndex                    0x2E                          /* or 0x4E */
#define    sioData                     0x2F                          /* or 0x4F */

/*-----   routing, sub-routing -----*/
void main()
{
    int iData;

    SioGPIOMode(0x0F);
    delay(2000);

          SioGPIOData(0x05);
          delay(2000);

    iData = SioGPIOStatus();
    printf(" Input : %2x \n",iData);
    delay(2000);

          SioGPIOData(0x0A);
          delay(2000);

    iData = SioGPIOStatus();
    printf(" Input : %2x \n",iData);
    delay(2000);
}

void SioGPIOMode(int iMode)
{
    outportb(sioIndex,0x87);                                  /* Enable Super I/O */
    outportb(sioIndex,0x87);

    outportb(sioIndex,0x07);                                  /* Select logic device - GPIO */
    outportb(sioData, 0x06);

    outportb(sioIndex,0x30);                                  /* Enable GPIO */
    outportb(sioData, 0x01);

    outportb(sioIndex,0xC0);                                  /* GPIO3 0~7 - Output Enable */
    outportb(sioData,iMode);

          outportb(sioIndex,0xAA);                                    /* Disable Super I/O */
}


void SioGPIOData(int iData)
{
    outportb(sioIndex,0x87);                                  /* Enable Super I/O */
    outportb(sioIndex,0x87);
```

```
    outportb(sioIndex,0x07);                        /* Select logic device - GPIO */
    outportb(sioData, 0x06);

    outportb(sioIndex,0xC1);                        /* GPIO3 0~7 - Output Data */
    outportb(sioData,iData);

          outportb(sioIndex,0xAA);                          /* Disable Super I/O */
}


int SioGPIOStatus()
{
          int iStatus;

    outportb(sioIndex,0x87);                        /* Enable Super I/O */
    outportb(sioIndex,0x87);

    outportb(sioIndex,0x07);                        /* Select logic device - GPIO */
    outportb(sioData, 0x06);

          outportb(sioIndex,0xC2);                          /* GPIO3 0~7 - Status */
    iStatus = inportb(sioData);

          outportb(sioIndex,0xAA);                          /* Disable Super I/O */

          return iStatus;
}
```