MB-i87Q0

Micro-ATX Industrial Motherboard

User's Manual

Version 1.0

2014.01

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Revision History

Version	Release Time	Description
1.0	January 2014	Initial release

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Copyright Notice

The information in this document is subject to change without prior notice in order to improve the reliability, design and function. It does not represent a commitment on the part of the manufacturer.

Under no circumstances will the manufacturer be liable for any direct, indirect, special, incidental, or consequential damages arising from the use or inability to use the product or documentation, even if advised of the possibility of such damages.

Declaration of Conformity

CE

The CE symbol on your product indicates that it is in compliance with the directives of the Union European (EU). A Certificate of Compliance is available by contacting Technical Support.

This product has passed the CE test for environmental specifications when shielded cables are used for external wiring. We recommend the use of shielded cables. This kind of cable is available from ARBOR. Please contact your local supplier for ordering information.

This product has passed the CE test for environmental specifications. Test conditions for passing included the equipment being operated within an industrial enclosure. In order to protect the product from being damaged by ESD (Electrostatic Discharge) and EMI leakage, we strongly recommend the use of CE-compliant industrial enclosure products.

Warning

This is a class B product. In a domestic environment this product may cause radio interference in which case the user may be required to take adequate measures.

FCC Class B

This device complies with Part 15 of the FCC Rules. Operation is subject to the following two conditions:

(1) This device may not cause harmful interference, and

(2) This device must accept any interference received, including interference that may cause undesired operation.

NOTE:

This equipment has been tested and found to comply with the limits for a Class B digital device, pursuant to Part 15 of the FCC Rules. These limits are designed to provide reasonable protection against harmful interference when the equipment is operated in a commercial environment. This equipment generates, uses, and can radiate radio frequency energy and, if not installed and used in accordance with the instruction manual, may cause harmful interference to radio communications. Operation of this equipment in a residential area is likely to cause harmful interference in which case the user will be required to correct the interference at his own expense.

RoHS

ARBOR Technology Corp. certifies that all components in its products are in compliance and conform to the European Union's Restriction of Use of Hazardous Substances in Electrical and Electronic Equipment (RoHS) Directive 2002/95/EC.

The above mentioned directive was published on 2/13/2003. The main purpose of the directive is to prohibit the use of lead, mercury, cadmium, hexavalent chromium, polybrominated biphenyls (PBB), and polybrominated diphenyl ethers (PBDE) in electrical and electronic products. Member states of the EU are to enforce by 7/1/2006.

ARBOR Technology Corp. hereby states that the listed products do not contain unintentional additions of lead, mercury, hex chrome, PBB or PBDB that exceed a maximum concentration value of 0.1% by weight or for cadmium exceed 0.01% by weight, per homogenous material. Homogenous material is defined as a substance or mixture of substances with uniform composition (such as solders, resins, plating, etc.). Lead-free solder is used for all terminations (Sn(96-96.5%), Ag(3.0-3.5%) and Cu(0.5%)).

SVHC / REACH

To minimize the environmental impact and take more responsibility to the earth we live, Arbor hereby confirms all products comply with the restriction of SVHC (Substances of Very High Concern) in (EC) 1907/2006 (REACH --Registration, Evaluation, Authorization, and Restriction of Chemicals) regulated by the European Union.

All substances listed in SVHC < 0.1 % by weight (1000 ppm)

Warning

Single Board Computers and their components contain very delicate Integrated Circuits (IC). To protect the Single Board Computer and its components against damage from static electricity, you should always follow the following precautions when handling it :

1. Disconnect your Single Board Computer from the power source when you want to work on the inside.
2. Hold the board by the edges and try not to touch the IC chips, leads or circuitry.
3. Use a grounded wrist strap when handling computer components.
4. Place components on a grounded antistatic pad or on the bag that comes with the Single Board Computer, whenever components are separated from the system.

Replacing Lithium Battery

Incorrect replacement of the lithium battery may lead to a risk of explosion.

The lithium battery must be replaced with an identical battery or a battery type recommended by the manufacturer.

Do not throw lithium batteries into the trash-can. It must be disposed of in accordance with local regulations concerning special waste.

Technical Support

If you have any technical difficulties, please do not hesitate to call or e-mail our customer service.

http://www.arbor.com.tw

E-mail:info@arbor.com.tw

Warranty

This product is warranted to be in good working order for a period of two years from the date of purchase. Should this product fail to be in good working order at any time during this period, we will, at our option, replace or repair it at no additional charge except as set forth in the following terms. This warranty does not apply to products damaged by misuse, modifications, accident or disaster.

Vendor assumes no liability for any damages, lost profits, lost savings or any other incidental or consequential damage resulting from the use, misuse of, or inability to use this product. Vendor will not be liable for any claim made by any other related party.

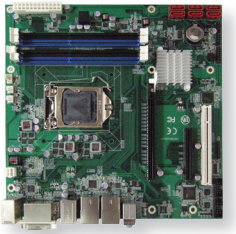
Vendors disclaim all other warranties, either expressed or implied, including but not limited to implied warranties of merchantability and fitness for a particular purpose, with respect to the hardware, the accompanying product's manual(s) and written materials, and any accompanying hardware. This limited warranty gives you specific legal rights.

Return authorization must be obtained from the vendor before returned merchandise will be accepted. Authorization can be obtained by calling or faxing the vendor and requesting a Return Merchandise Authorization (RMA) number. Returned goods should always be accompanied by a clear problem description.

Chapter 1

Introduction

1.1. Product Highlights



- Intel® 4th Gen. Core™ Processors in LGA1150 supported
- Dual GbE ports
- DVI-I and DisplayPort supported
- RS-485 Auto-flow Control supported
- Intel® AMT supported
- RAID 0, 1, 5, 10 supported
- USB 3.0 supported

1.2. About this Manual

This manual is intended for experienced users and integrators with hardware knowledge of computers. If you are not sure about the description in this manual, consult your vendor before further handling.

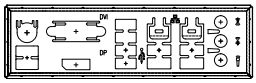
We recommend that you keep one copy of this manual for the quick reference for any necessary maintenance in the future. Thank you for choosing ARBOR products.

1.3. Specifications

Form Factor	Micro-ATX Industrial Motherboard
CPU	Intel® 4th Generation Core™ i7/i5/i3 and Pentium® / Celeron® processors in LGA1150 socket
Chipset	Intel® Q87 PCH
System Memory	4 x DDR3 Long-DIMM sockets, supporting 1600MT/s SDRAM up to 32GB
Display	Integrated Intel® HD Graphics • 1 x DVI-I connector • 1 x DisplayPort 1.2a
Ethernet	1 x Intel® PCIe i217LM GbE PHY (iAMT supported)
	1 x Intel® PCIe i210AT GbE controller
I/O Chip	Fintek F71869ED
BIOS	AMI BIOS
Watchdog Timer	1~255 levels reset
Serial ATA	6 x serial ATA ports with 600MB/s HDD transfer rate RAID 0, 1, 5, 10 supported
Serial Port	2 x COM ports (RS-232/422/485 selectable)
Universal Serial Bus	10 x USB 2.0 ports
	4 x USB 3.0/2.0 ports,
KB/MS	1 x 6-pin mini-DIN connector for PS/2 keyboard, and mouse via Y-cable
Expansion Bus	1 x PCIe x16 slot 1 x PCIe x4 interface x8 slot 1 x PCI slot
Digital I/O	1 x 16-bit digital IO, 8-bit input/ 8-bit output
Audio	Realtek ALC662 HD Audio CODEC, MIC-in/ Line-out
Power Connector	1 x 24-pin ATX power connector
	1 x 4-pin 12V ATX power connector
Operating Temp.	0ºC ~ 60ºC (32ºF ~ 140ºF)
Storage Temp.	-20ºC ~ 80ºC (-4ºF ~ 176ºF)
Humidity	10 ~ 95% @ 60ºC (non-condensing)
Dimension (L x W)	244 x 244 mm (9.6” x 9.6”)

1.4. Inside the Package

Before starting to install the single board, make sure the following items are shipped:

	1 x MB-i87Q0 Industrial Motherboard
	1 x Driver CD
	1 x Quick Installation Guide
	1 x I/O Bracket

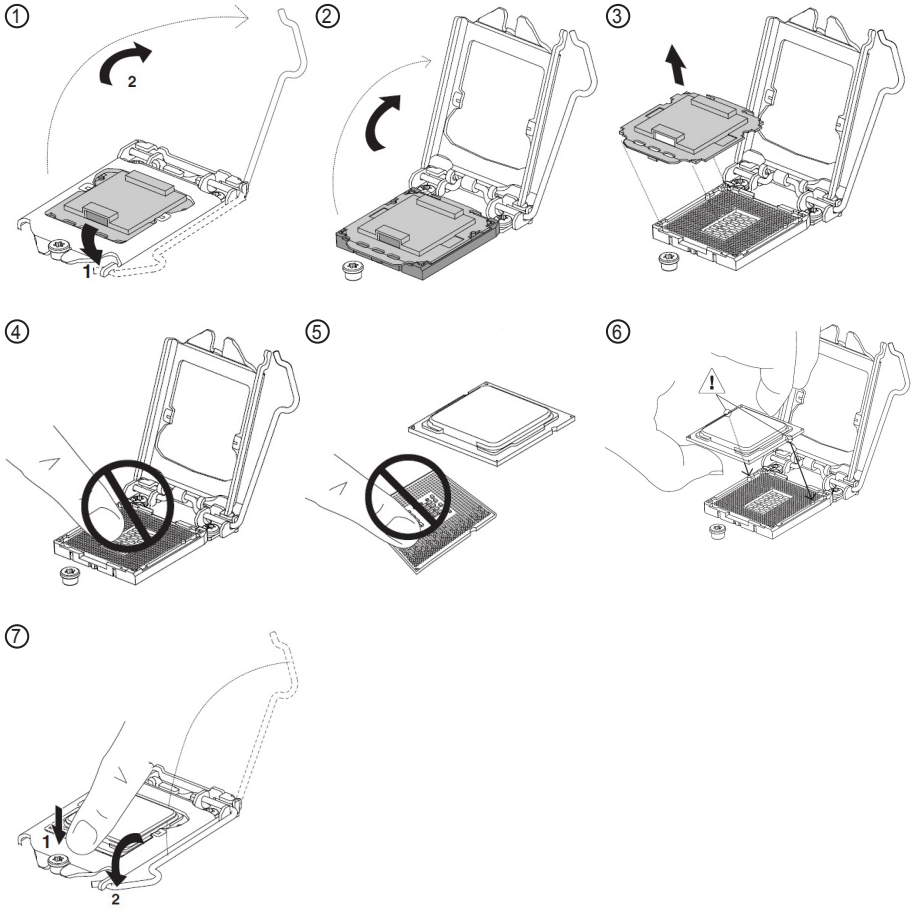
If any of the aforelisted items is damaged or missing, contact your vendor immediately.

1.5. Ordering Information

MB-i87Q0	Intel® 4th Gen. Core™ Embedded Micro-ATX Motherboard
CPF-67Q0-C1	CPU Colling Fan for LGA1150/ 1155/ 1156 CPU
CBK-10-87Q0-00	Cable kit 1 x two-port COM cable 2 x USB cables 6 x SATA cables 1 x PS/2 Y-cable

1.6. CPU Installation

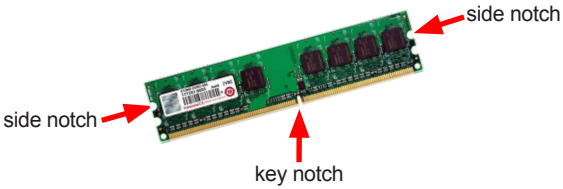
The LGA1150 processor socket comes with a lever to secure the processor. Please refer to the pictures step by step as below and note that the cover of the LGA1155 socket must always be installed during transportation to avoid damage to the socket.



Make sure that heat sink putting on the CPU's top surface is in complete contact to avoid overheating problem.
If not, it would cause your system or CPU hanged, unstable or damaged.

1.7. RAM Installation

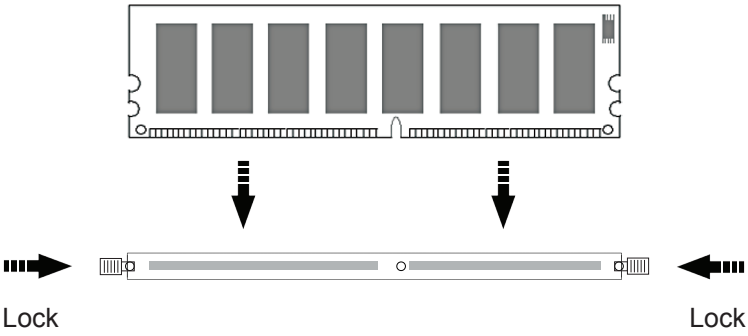
The main board has one dual inline memory module (DIMM) sockets. Load the computer with a memory module of higher capacity to make programs run faster. The memory module for the computer's Long DIMM socket should be a 240-pin DDR3 with a "key notch" off the centre among the pins, which enables the memory module for particular applications. There are another two notches at each left and right side of the memory module to help fix the module in the socket.



To install the memory module:

1. Find the DIMM socket on the board as marked in the illustration below. The DIMM socket is horizontal type, and it has two spring-loaded locks to fix the memory module.

2. Confront the memory module's edge connector with the DIMM slot connector. Align the memory module's key notch at the break on the DIMM slot connector.



3. Fully plug the memory module until it gets auto-locked in place.

To uninstall the memory module:

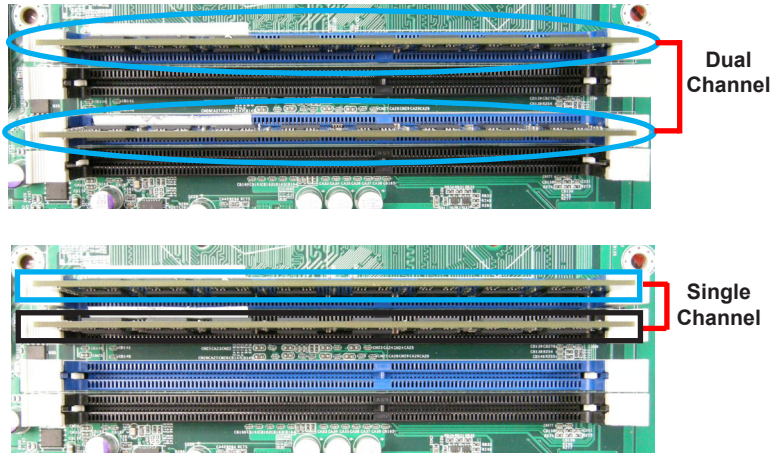
1. Pull back the locks from both sides of the DIMM socket.
   The memory module will be auto-released from the socket.
2. Remove the memory module.

Rules to enable dual-channel mode

To achieve dual-channel mode, the following conditions must be met:

- **Same memory size**. Examples: 1 GB, 2 GB, 4 GB.
- **Matched DIMM configuration in each channel**, Ex. Single-sided/Double -sided, SDRAM Organization Front-side/Back-side, or SDRAM Density
- **Matched in symmetrical memory slots** (see the illustration as below)

Configurations that do not match the above conditions revert to single-channel mode.



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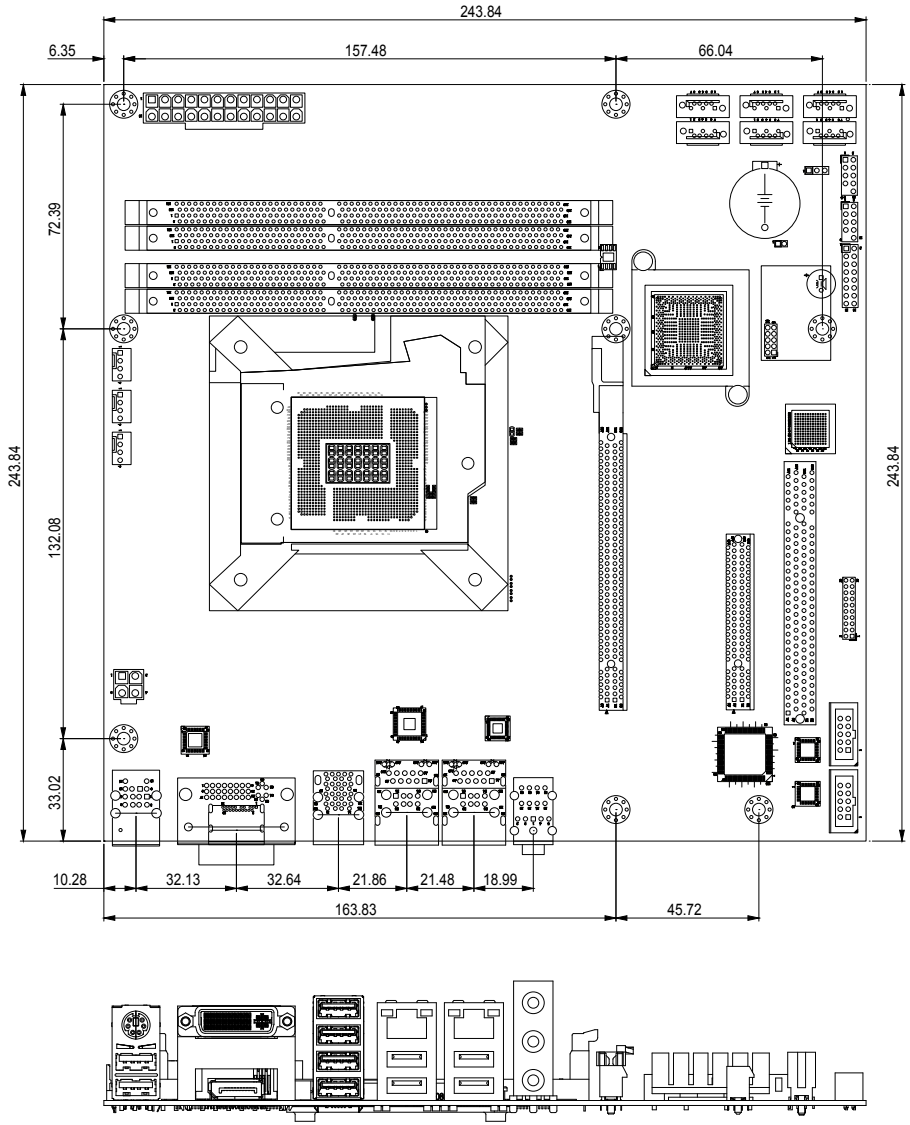
Chapter 2

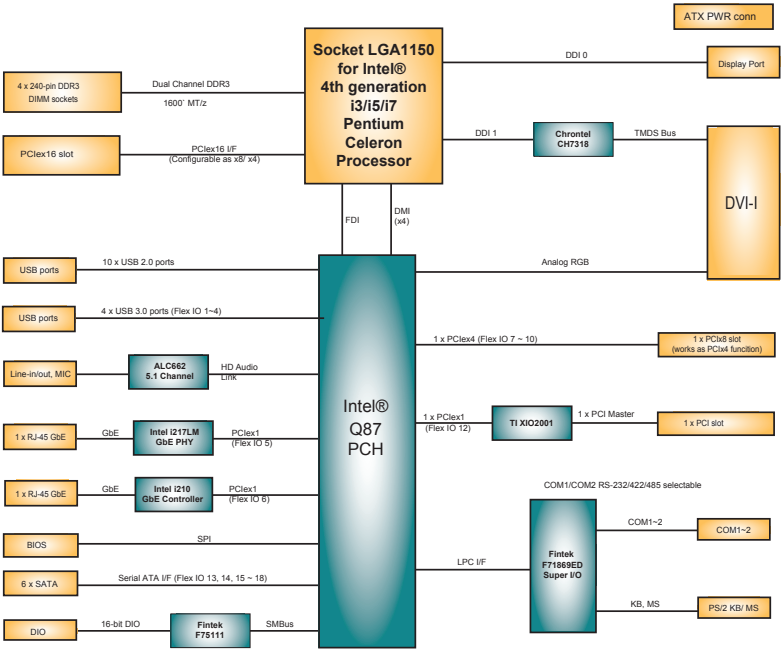
Getting Started

2.1. Board Dimensions



Unit: mm

2.2. Block Diagram

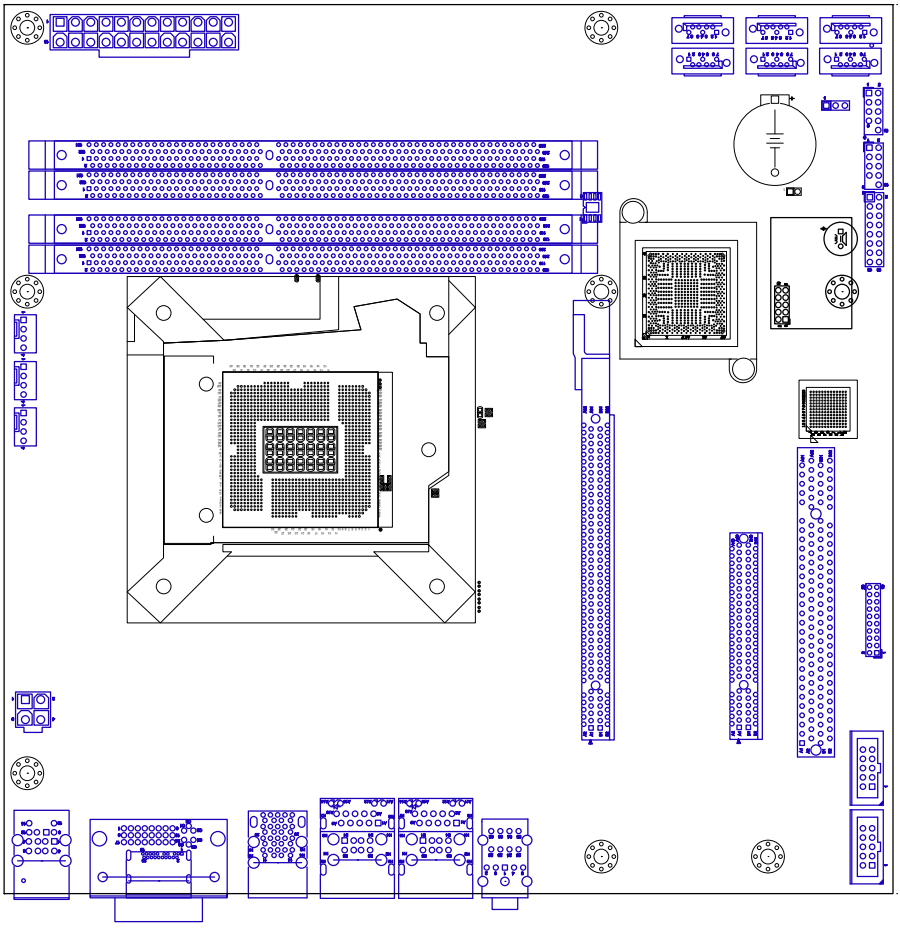


2.3. Jumpers & Connectors

The board comes with some connectors to join some devices and also some jumpers to alter the hardware configuration. The following in this chapter will explicate each of these components one-by-one.

2.3.1. Layout

This section will provide an overview of this board.



2.3.2. Jumpers

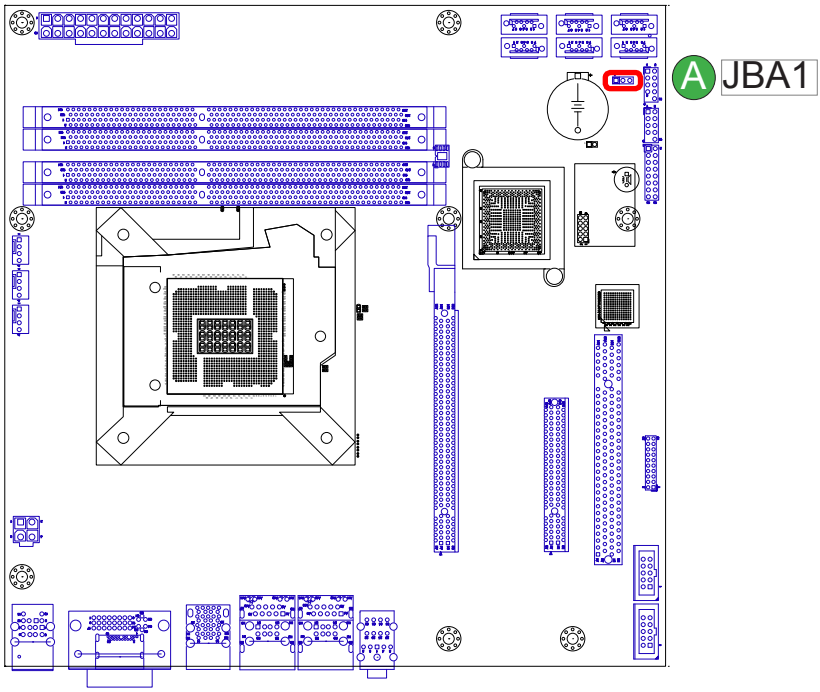
JBAT1

Function:	Clears/keeps CMOS
Jumper Type:	2.54mm pitch 1x3-pin header

Setting:

Pin	Description	
1-2	Keeps CMOS (default)	
2-3	Clears CMOS	

Board Top



2.3.3. Connectors

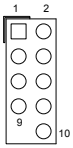
USB2,3

Function: Connectors for USB 2.0 ports

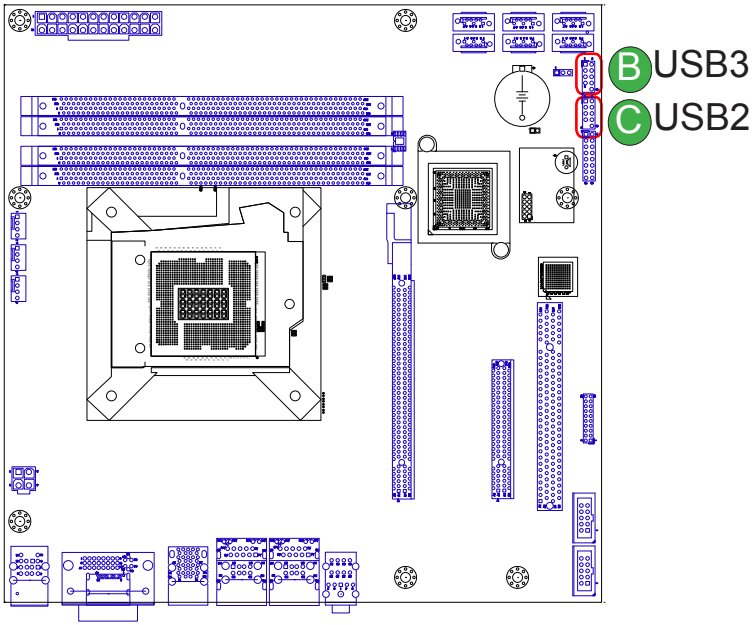
Connector Type: 2.54mm pitch 10-pin header

Pin Assignment:

Pin	Description	Pin	Description
1	+5V(A)	2	+5V(B)
3	USBD-(A)	4	USBD-(B)
5	USBD+(A)	6	USBD+(B)
7	GND(A)	8	GND(B)
9	N/C(A)	10	GND(B)



Board Top



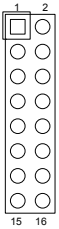
JFRT1

Function: Connectors for front-panel switches and LED status lamps

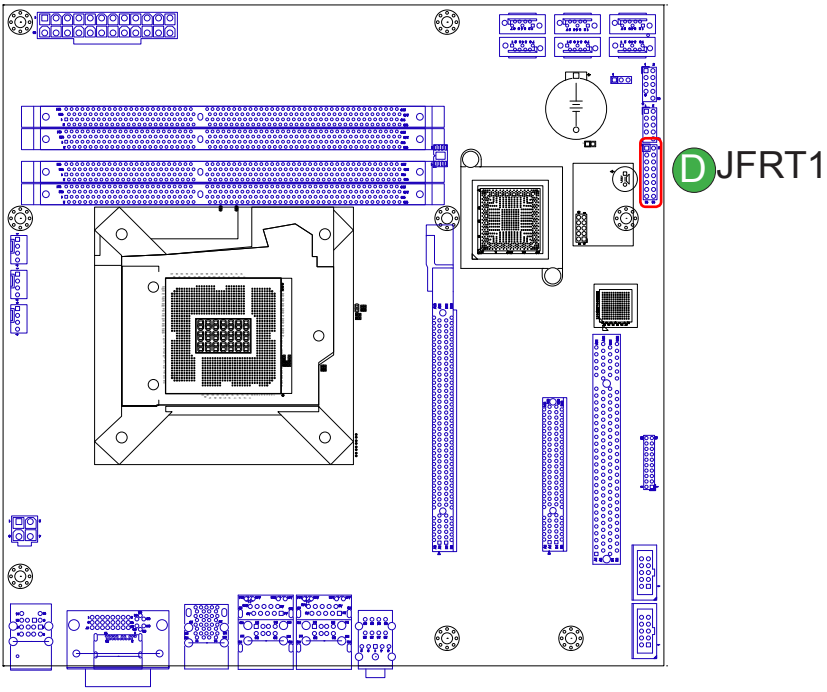
Connector Type: 2.54mm pitch 2x8-pin header

Pin Assignment:

Pin	Description	Pin	Description
1	P_LED+	2	PWR_BTN+
3	P_LED-	4	PWR_BTN-
5	P_LED-	6	RESET+
7	HDD_LED+	8	RESET-
9	HDD_LED-	10	SPK+
11	SMB(CLK)	12	SPK+
13	SMB(DAT)	14	SPK-
15	SMB(G)	16	SPK-



Board Top



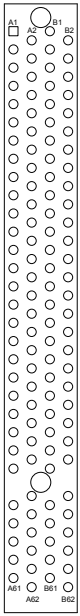
PCI1

Function: PCI connector

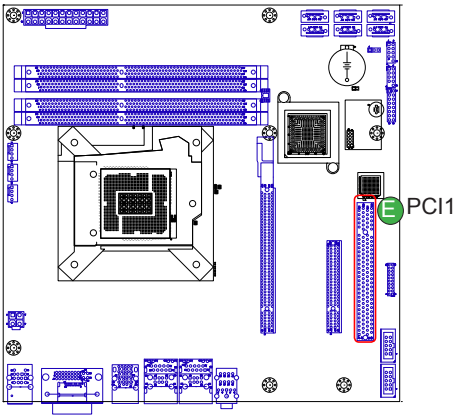
Connector Type: 32-bit PCI slot

Setting:

Pin	Desc.	Pin	Desc.	Pin	Desc.	Pin	Desc.
A1	TRST	A2	+12V	B1	-12V	B2	TCK
A3	TMS	A4	TDI	B3	GND	B4	TDO
A5	+5V	A6	INTA#	B5	+5V	B6	+5V
A7	INTC#	A8	+5V	B7	INTB#	B8	INTD#
A9	RSVD	A10	+5V	B9	PRSTN1	B10	RSVD
A11	RSVD	A12	GND	B11	PRSTN2	B12	GND
A13	GND	A14	3.3V_AUX	B13	GND	B14	RSVD
A15	RST#	A16	+5V	B15	GND	B16	CLK
A17	GNT#	A18	GND	B17	GND	B18	REQ#
A19	PME#	A20	AD30	B19	+5V	B20	AD31
A21	+3.3V	A22	AD28	B21	AD29	B22	GND
A23	AD26	A24	GND	B23	AD27	B24	AD25
A25	AD24	A26	IDSEL	B25	+3.3V	B26	C/BE3#
A27	+3.3V	A28	AD22	B27	AD23	B28	GND
A29	AD20	A30	GND	B29	AD21	B30	AD19
A31	AD18	A32	AD46	B31	+3.3V	B32	AD17
A33	+3.3V	A34	FRAME#	B33	C/BE2#	B34	GND
A35	GND	A36	TRDY#	B35	IRDY#	B36	+3.3V
A37	GND	A38	STOP#	B37	DEV-SEL#	B38	GND
A39	+3.3V	A40	SDONE	B39	LOCK#	B40	PERR#
A41	SBO#	A42	GND	B41	+3.3V	B42	SERR#
A43	PAR	A44	AD15	B43	+3.3V	B44	C/BE1#
A45	+3.3V	A46	AD13	B45	AD14	B46	GND
A47	AD11	A48	GND	B47	AD12	B48	AD10
A49	AD9	A52	C/BE0#	B49	GND	B52	AD6
A53	+3.3V	A54	AD6	B53	AD7	B54	+3.3V
A55	AD4	A56	GND	B55	AD5	B56	AD3
A57	AD2	A58	AD0	B57	GND	B58	AD1
A59	+5V	A60	REQ64#	B59	+5V	B60	ACK64#
A61	+5V	A62	+5V	B61	+5V	B62	+5V



Board Top



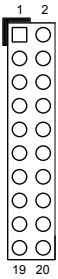
JDIO1

Function: Digital I/O connector

Connector Type: 2.54mm pitch 2x10-pin header

Pin Assignment:

Pin	Description	Pin	Description
1	DIO_OUT_0	2	DIO_OUT_1
3	DIO_OUT_2	4	DIO_OUT_3
5	DIO_OUT_4	6	DIO_OUT_5
7	DIO_OUT_6	8	DIO_OUT_7
9	DIO_IN_0	10	DIO_IN_1
11	DIO_IN_2	12	DIO_IN_3
13	DIO_IN_4	14	DIO_IN_5
15	DIO_IN_6	16	DIO_IN_7
17	VCC5	18	GND
19	VCC5	20	GND



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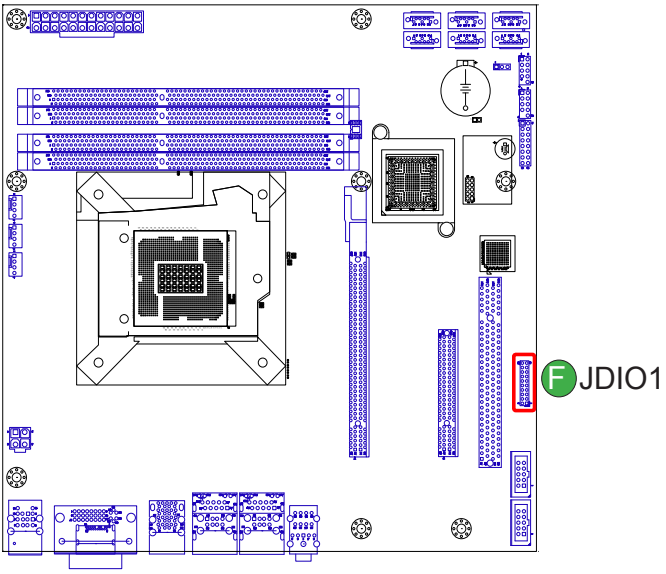


JCOM1,2

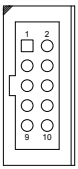
Function: Connectors for RS-232, RS422, RS485 serial ports

Connector Type: 2.54mm pitch 2x5-pin box heade

Pin Assignment:

RS232 Mode:

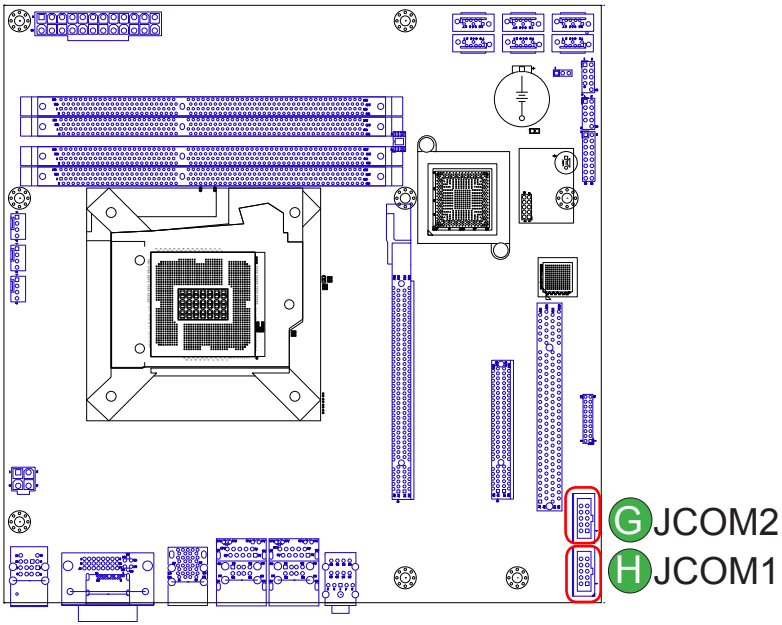
Pin	Description	Pin	Description
1	DCD	6	DSR
2	RXD	7	RTS
3	TXD	8	CTS
4	DTR	9	RI
5	GND	10	GND



RS422 Mode:		RS485 Mode:	
Pin	Description	Pin	Description
1	TX-	1	TX- or RX-
3	TX+	3	TX+ or RX+
5	RX+		
7	RX-		

To configure the data transmission interface for the available serial ports, access BIOS Setup utility | Advanced | F71869E Super IO Configuration | Serial Port 1 & 2 Configuration.

Board Top



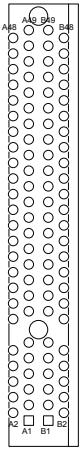
PCIE1

Function: PCI Express connector

Connector Type: PCI Express x8 slot with x4 single

Pin Assignment:

Pin	Desc.	Pin	Desc.
B1	-12V	A1	TRST
B2	TCK	A2	+12V
B3	GND	A3	TMS
B4	TDO	A4	TDI
B5	+5V	A5	+5V
B6	+5V	A6	INTA#
B7	INTB#	A7	INTC#
B8	INTD#	A8	+5V
B9	PRSTN1	A9	RSVD
B10	RSVD	A10	+5V
B11	PRSTN2	A11	RSVD
B12	GND	A12	GND
B13	GND	A13	GND
B14	RSVD	A14	3.3V_AUX
B15	GND	A15	RST#
B16	CLK	A16	+5V
B17	GND	A17	GNT#
B18	REQ#	A18	GND
B19	+5V	A19	PME#
B20	AD31	A20	AD30
B21	AD29	A21	+3.3V
B22	GND	A22	AD28
B23	AD27	A23	AD26
B24	AD25	A24	GND
B25	+3.3V	A25	AD24
B26	C/BE3#	A26	IDSEL
B27	AD23	A27	+3.3V
B28	GND	A28	AD22
B29	AD21	A29	AD20
B30	AD19	A30	GND
B31	+3.3V	A31	AD18
B32	AD17	A32	AD46



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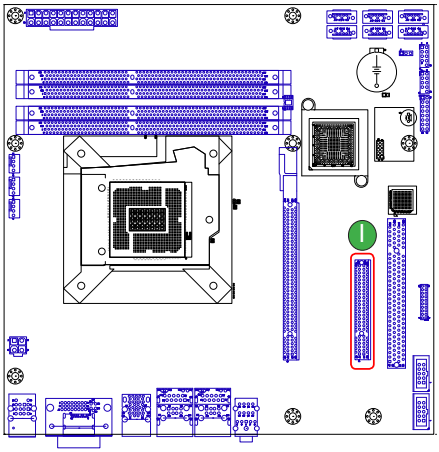


I:PCIE1

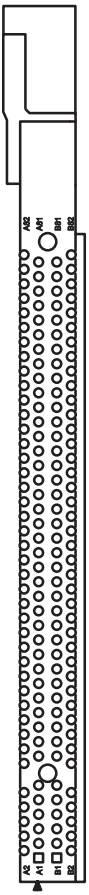
PCIE2

Function: PCI Express connector

Connector Type: PCI Express x16 slot

Pin Assignment:

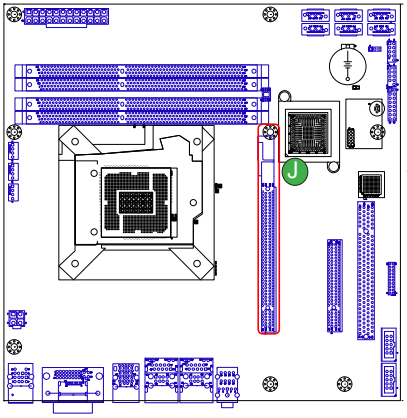
Pin	Desc.	Pin	Desc.
B1	+12V	A1	PRSNT1
B2	+12V	A2	+12V
B3	+12V	A3	+12V
B4	GND	A4	GND
B5	SMCLK	A5	JTAG2
B6	SMDAT	A6	JTAG3
B7	GND	A7	JTAG4
B8	+3.3V	A8	JTAG5
B9	JTAG1	A9	+3.3V
B10	+3.3VAUX	A10	+3.3V
B11	WAKE#	A11	PWRGD
B12	RSVD	A12	GND
B13	GND	A13	REFCLK+
B14	PEG_C_TX0+	A14	REFCLK-
B15	PEG_C_TX0-	A15	GND
B16	GND	A16	PEG_RX0+
B17	PRSNT2	A17	PEG_RX0-
B18	GND	A18	GND
B19	PEG_C_TX1+	A19	RSVD
B20	PEG_C_TX1-	A20	GND
B21	GND	A21	PEG_RX1+
B22	GND	A22	PEG_RX1-
B23	PEG_C_TX2+	A23	GND
B24	PEG_C_TX2-	A24	GND
B25	GND	A25	PEG_RX2+
B26	GND	A26	PEG_RX2-
B27	PEG_C_TX3+	A27	GND



Pin	Desc.	Pin	Desc.
B28	PEG_C_TX3-	A28	GND
B29	GND	A29	PEG_RX3+
B30	RSVD	A30	PEG_RX3-
B31	PRSNT2	A31	GND
B32	GND	A32	RSVD
B33	PEG_C_TX4+	A33	RSVD
B34	PEG_C_TX4-	A34	GND
B35	GND	A35	PEG_RX4+
B36	GND	A36	PEG_RX4-
B37	PEG_C_TX5+	A37	GND
B38	PEG_C_TX5-	A38	GND
B39	GND	A39	PEG_RX5+
B40	GND	A40	PEG_RX5-
B41	PEG_C_TX6+	A41	GND
B42	PEG_C_TX6-	A42	GND
B43	GND	A43	PEG_RX6+
B44	GND	A44	PEG_RX6-
B45	PEG_C_TX7+	A45	GND
B46	PEG_C_TX7-	A46	GND
B47	GND	A47	PEG_RX7+
B48	PRSNT2	A48	PEG_RX7-
B49	GND	A49	GND
B50	PEG_C_TX8+	A50	RSVD
B51	PEG_C_TX8-	A51	GND
B52	GND	A52	PEG_RX8+
B53	GND	A53	PEG_RX8-
B54	PEG_C_TX9+	A54	GND
B55	PEG_C_TX9-	A55	GND
B56	GND	A56	PEG_RX9+
B57	GND	A57	PEG_RX9-
B58	PEG_C_TX10+	A58	GND
B59	PEG_C_TX10-	A61	GND
B60	GND	A62	PEG_RX10+
B61	GND	A61	PEG_RX10-

Pin	Desc.	Pin	Desc.
B62	PEG_C_TX11+	A62	GND
B63	PEG_C_TX11-	A63	GND
B64	GND	A64	PEG_RX11+
B65	GND	A65	PEG_RX11-
B66	PEG_C_TX12+	A66	GND
B67	PEG_C_TX12-	A67	GND
B68	GND	A68	PEG_RX12+
B69	GND	A69	PEG_RX12-
B70	PEG_C_TX13+	A70	GND
B71	PEG_C_TX13-	A71	GND
B72	GND	A72	PEG_RX13+
B73	GND	A73	PEG_RX13-
B74	PEG_C_TX14+	A74	GND
B75	PEG_C_TX14-	A75	GND
B76	GND	A76	PEG_RX14+
B77	GND	A77	PEG_RX14-
B78	PEG_C_TX15+	A78	GND
B79	PEG_C_TX15-	A79	GND
B80	GND	A80	PEG_RX15+
B81	PRSNT2	A81	PEG_RX15-
B82	RSVD	A82	GND

Board Top



J:PCIE2

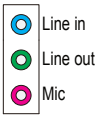
AUDIO1

Function: Audio interface ports

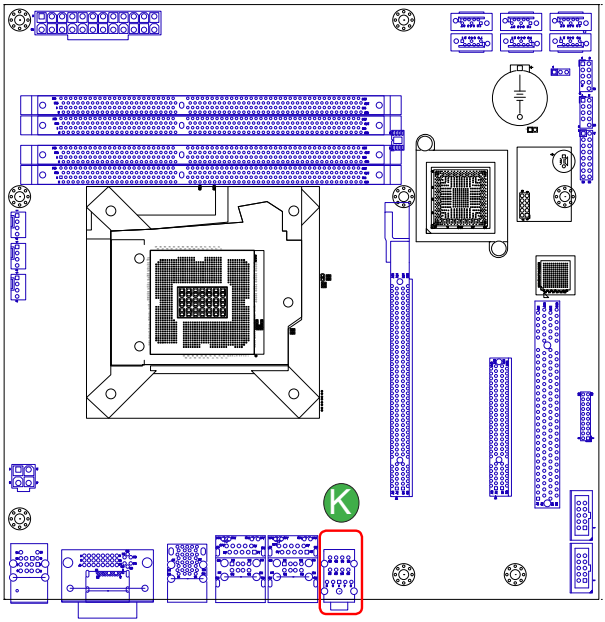
Connector Type: Triple-stacked ø3.5mm stereo audio jacks

Pin Assignment:

Audio Jack	Description
Blue	Line-in
Green	Line-out
Pink	Mic-in



Board Top



K:AUDIO1

JLAN1,2

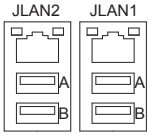
Function: RJ-45+USB stacked ports

Connector Type: RJ-45 LAN port with LED lamps and double-stacked USB 2.0 Type A connectors

Pin Assignment:

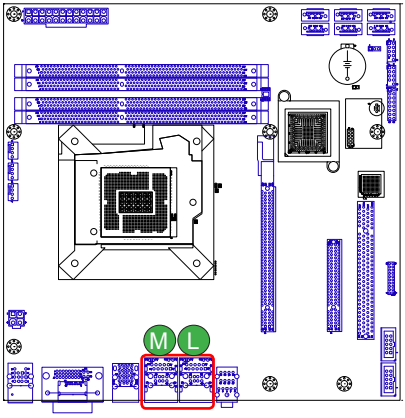
LAN (RJ-45)

LED	Definition
Speed	Amber:1000M Green: 10/100M
Link/Act	On: Linked Blink: Network Activity Off: No Link



LAN (RJ-45)			
Pin	**Desc.**	**Pin**	**Desc.**
A1	TCT VCC	A2	M0+
A3	M0-	A4	M1+
A5	M1-	A6	M2+
A7	M2-	A8	M3+
A9	M3-	A10	RCT GND
A11	LED1 Y-	A12	LED1 Y+
A13	LED2 G-O+	A14	LED2 G+O-
USB (Type-A USB connector)			
B1	+5V (A)	B5	+5V (B)
B2	USBD1- (A)	B6	USBD2- (B)
B3	USBD1+ (A)	B7	USBD2+ (B)
B4	GND(A)	B8	GND (B)

Board Top



L:JLAN1
M:JLAN2

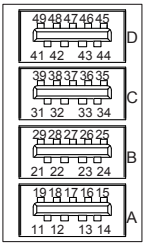
USB1

Function: 4 x USB3.0 ports

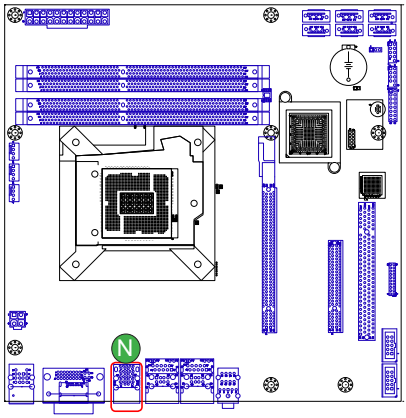
Connector Type: Quadruple-stacked USB 3.0 Type A connectors

Pin Assignment:

Pin	Desc.	Pin	Desc.
11	5V (A)	21	5V (B)
12	USBD1- (A)	22	USBD2- (B)
13	USBD1+ (A)	23	USBD2+ (B)
14	GND1 (A)	24	GND3 (B)
15	SSRX1- (A)	25	SSRX2- (B)
16	SSRX1+ (A)	26	SSRX2+ (B)
17	GND2 (A)	27	GND4 (B)
18	SSTX1- (A)	28	SSTX2- (B)
19	SSTX1+ (A)	29	SSTX2+ (B)
31	5V (C)	41	5V (D)
32	USBD3- (C)	42	USBD4- (D)
33	USBD3+ (C)	43	USBD4+ (D)
34	GND5 (C)	44	GND7 (D)
35	SSRX3- (C)	45	SSRX4- (D)
36	SSRX3+ (C)	46	SSRX4+ (D)
37	GND6 (C)	47	GND8 (D)
38	SSTX3- (C)	48	SSTX4- (D)
39	SSTX3+ (C)	49	SSTX4+ (D)



Board Top



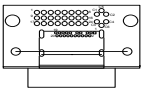
N:USB1

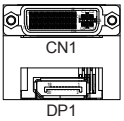
CN1 & DP1

Function: Stacked DVI-I connector and DisplayPort

Connector Type: Female DVI-I connector & DisplayPort 1.2 digital video connector

Pin Assignment:





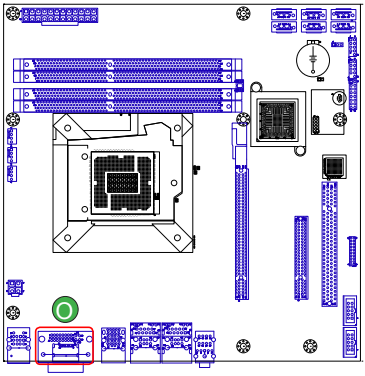
CN1

Pin	Description	Pin	Description	Pin	Description
1	DATA2-	13	DATA3+ (LINK1, NC)	C1	VGA Red
2	DATA2+	14	+5V	C2	VGA Green
3	DATA2/4 SHIELD	15	GND (for +5V)	C3	VGA Blue
4	DATA4- (LINK1, NC)	16	Hot Plug Detect	C4	VGA_H_Sync
5	DATA4+ (LINK1, NC)	17	DATA0-	C5	VGA_R,G,B_Return
6	DDC_CLK	18	DATA0+		
7	DDC_DATA	19	DATA0/5 SHIELD		
8	VGA_V_Sync	20	DATA5- (LINK1, NC)		
9	DATA1-	21	DATA5+ (LINK1, NC)		
10	DATA1+	22	Clock_SHIELD		
11	DATA1/3 SHIELD	23	Clock+		
12	DATA3- (LINK1, NC)	24	Clock-		

DP1

Pin	Description	Pin	Description	Pin	Description
1	LANE_0P	8	GND	15	GND
2	GND	9	LANE_2N	16	COM3_CTS#
3	LANE_0N	10	LANE_3P	17	AUX_N
4	LANE_1P	11	GND	18	HPD
5	GND	12	LANE_3N	19	RTN_PWR
6	LANE_1N	13	GND	20	PWR
7	LANE_2P	14	GND		

Board Top



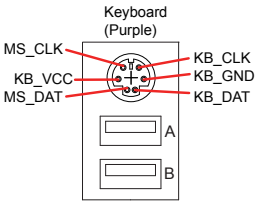
O:CN1 & DP1

KBUSB1

Function: Keyboard/mouse PS/2 and USB 2.0 stacked port

Connector Type: 6-pin Mini-DIN and Type A USB 2.0 stacked connectors

Pin Assignment:



USB (Type-A USB connector)

B1	+5V (A)	B5	+5V (B)
B2	USBD1- (A)	B6	USBD2- (B)
B3	USBD1+ (A)	B7	USBD2+ (B)
B4	GND(A)	B8	GND (B)

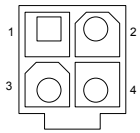
J1

Function: 12V ATX power supply connector

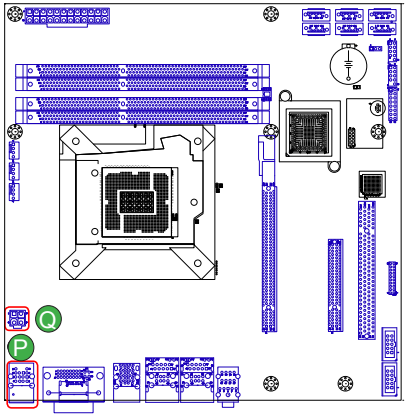
Connector Type: Standard 4-pin power connector

Pin Assignment:

Pin	Desc.
1	GND
2	GND
3	+12V
4	+12V



Board Top



P:KBUSB1
Q:J1

JFAN1, 2, 3

Function: Fan power connector

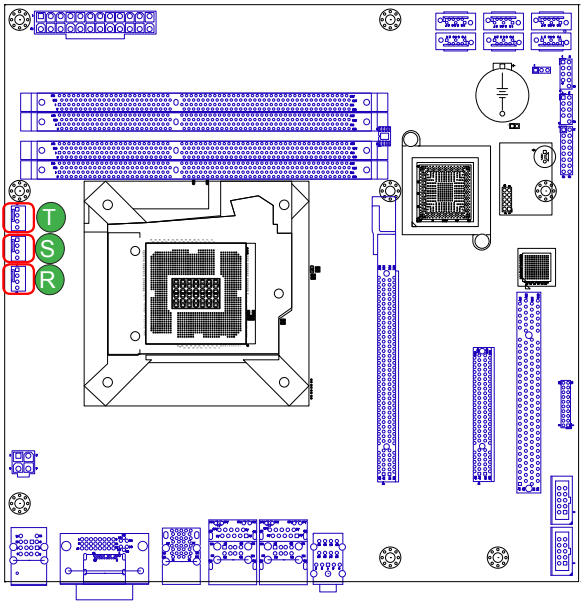
Connector Type: Onboard 1 x 4-pin one-wall wafer connector

Pin Assignment:

Pin	Description
1	GND
2	+12V
3	RPM
4	CTRL

Note: The fan must be a 12V fan.

Board Top



R:JFAN1
S:JFAN2
T:JFAN3

DIMM1,2,3,4

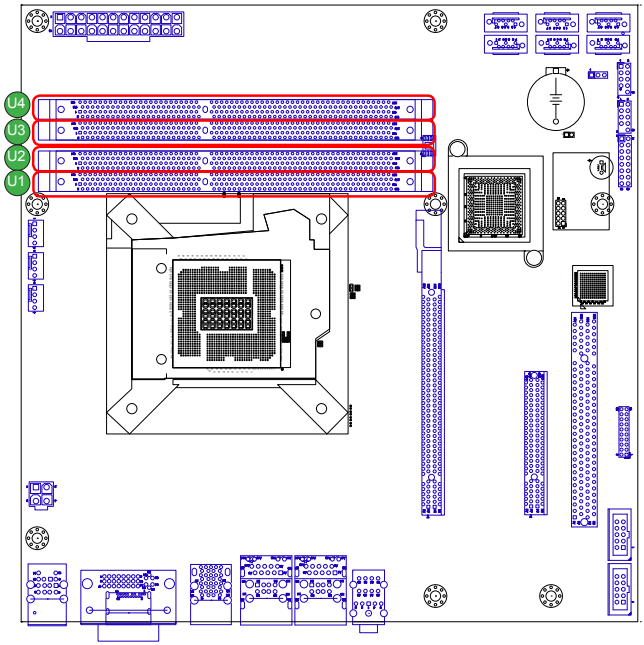
Function: **DDR3 DIMM connectors**

Connector Type: 240-pin DDR3 DIMM sockets

Pin Assignment:

Please visit the official consortium for the pin assignment.

Board Top



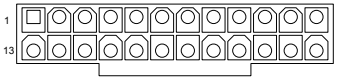
U1:DIMM1
U2:DIMM2
U3:DIMM3
U4:DIMM4

ATX1

Function: ATX power connector

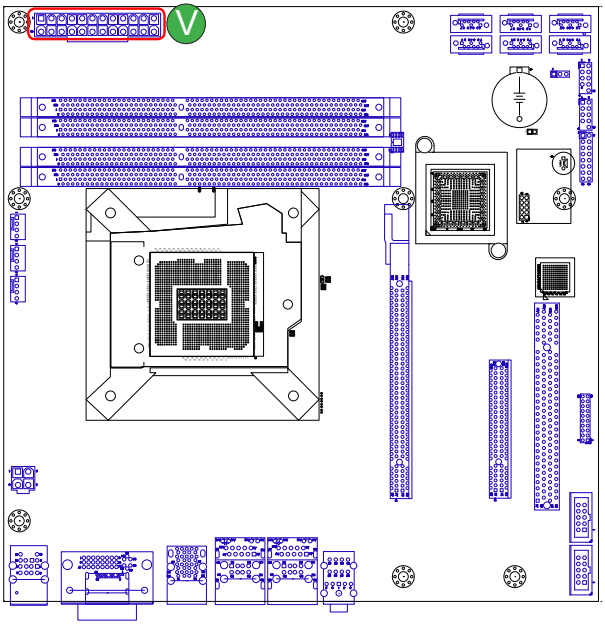
Connector Type: 24-pin ATX power supply connector

Pin Assignment:



Pin	Desc.	Pin	Desc.	Pin	Desc.
1	+3.3V	9	+5VSB	17	GND
2	+3.3V	10	+12V	18	GND
3	GND	11	+12V	19	GND
4	+5V	12	+3.3V	20	-5V
5	GND	13	+3.3V	21	+5V
6	+5V	14	-12V	22	+5V
7	GND	15	GND	23	+5V
8	PW-OK	16	PS-ON	24	GND

Board Top



V:ATX1

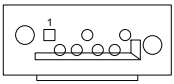
SATA1,2,3,4,5,6

Function: Serial ATA Connectors

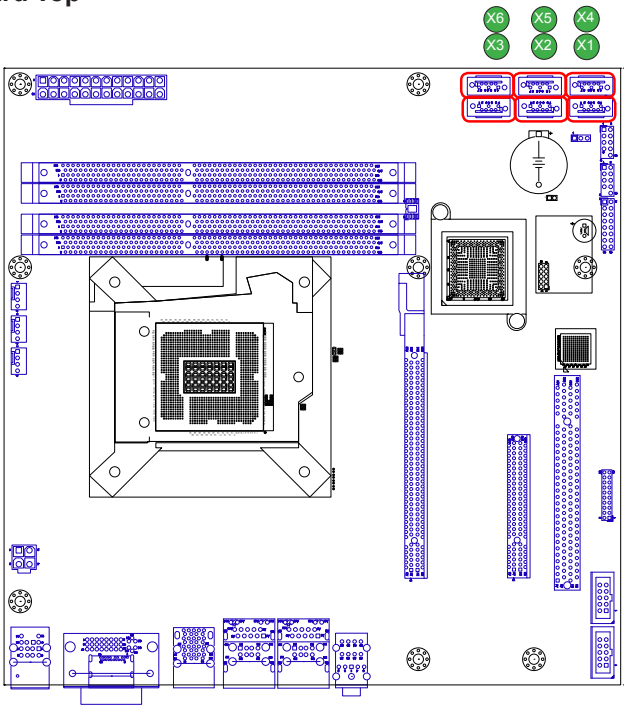
Connector Type: Lockable SATA connectors with housing, supporting 600MB/s HDD transfer rate.

Pin Assignment:

Pin	Desc.	Pin	Desc.
1	GND	2	TXP
3	TXN	4	GND
5	RXN	6	RXP
7	GND		



Board Top



X1:SATA1
X2:SATA2
X3:SATA3
X4:SATA4
X5:SATA5
X6:SATA6

2.4. Driver Installation Notes

The board supports Windows XP, Windows 7 and Windows 8. Find the necessary drivers on the CD that comes with your purchase. For different OS, the driver/utility installation may vary slightly, but generally they are similar. **DO** follow the sequence below to install all drivers to prevent errors:

Chipset→.NET Framework→Graphics→Audio→LAN→ME→Intel® Turbo→USB3.0

Find the drivers on CD by the following paths:

Windows 7

Device	Driver Path
Chipset	\MB-i87Q0\Chipset
VGA	\MB-i87Q0\Graphic\Win32_V9.18.10.3107
	\MB-i87Q0\Graphic\Win64_153117
LAN	\MB-i87Q0\Ethernet\Win7
Audio	\MB-i87Q0\AUDIO
Management Engine	\MB-i87Q0\ME\32bits_ME9.0_5M_V9.0.2.1345
	\MB-i87Q0\ME\64bits\WIN7
USB3.0	\MB-i87Q0\USB3.0\32bits_USB3_V2.5.0.19
	\MB-i87Q0\USB3.0\64bits_USB_3.0_Win7_2.5.1.28

Windows 8

Device	Driver Path
Chipset	\MB-i87Q0\Chipset
VGA	\MB-i87Q0\Graphic\Win32_V9.18.10.3107
	\MB-i87Q0\Graphic\Win64_153117
LAN	\MB-i87Q0\Ethernet\Win8
Audio	\MB-i87Q0\AUDIO
Management Engine	\MB-i87Q0\ME\32bits_ME9.0_5M_V9.0.2.1345
	\MB-i87Q0\ME\64bits\WIN8\MEI_Win8.1_5.0M_9.5.15.1730_PV

Chapter 3

BIOS

The BIOS Setup utility is featured by AMI BIOS to configure the system settings stored in the system's BIOS ROM. AMI BIOS is activated once the computer powers on.

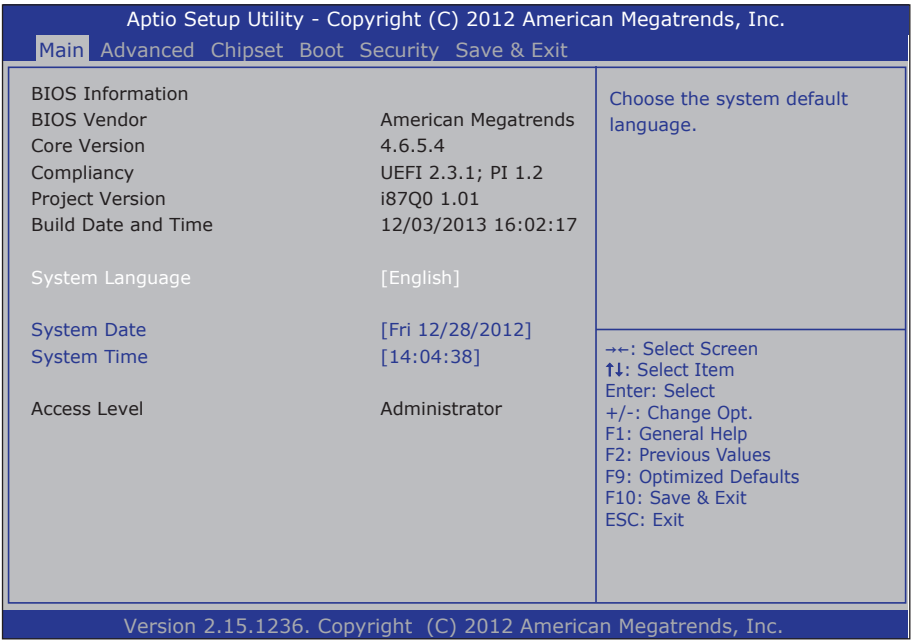
After entering the utility, use the left/right arrow keys to navigate between the top menus and use the down arrow key to access one.

Menu	Description
Main	See 3.1. Main on page 35.
Advanced	See 3.2. Advanced on page 36.
Chipset	See 3.3. Chipset on page 50.
Boot	See 3.4. Boot on page 35.
Security	See 3.5. Security on page 61.
Exit	See 3.6. Save & Exit on page 63.

NOTE: For system stability and performance, this BIOS utility is constantly improved. The screenshots demonstrated and descriptions hereinafter are for reference only and may not exactly meet what is presented onscreen.

3.1. Main

The **Main** menu displays some BIOS info and features the settings of **System Date** and **System Time**.



The BIOS info displayed is:

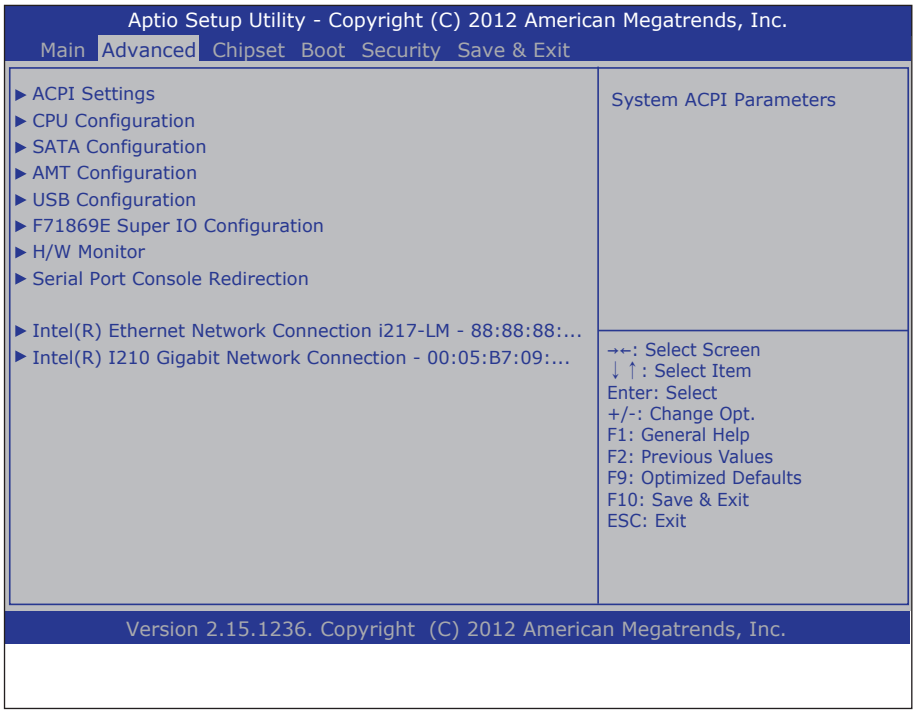
Info Item	Description
BIOS Vendor	Delivers the provider of the BIOS Setup utility.
Core Version	Delivers the version of the core.
BIOS Version	Delivers the computer's BIOS version.
Compliancy	Delivers the UEFI support.
Project Version	Delivers the board's BIOS version.
Build Date and Time	Delivers the date and time the BIOS Setup utility was made/updated.
Access Level	Delivers the level by which the BIOS Setup utility is being accessed at the moment.

The featured settings are:

Setting	Description
System Time	Sets system time.
System Date	Sets system date.

3.2. Advanced

The **Advanced** menu controls the system's CPU, IDE, Super IO, SATA and USB. It also helps users monitor hardware health.

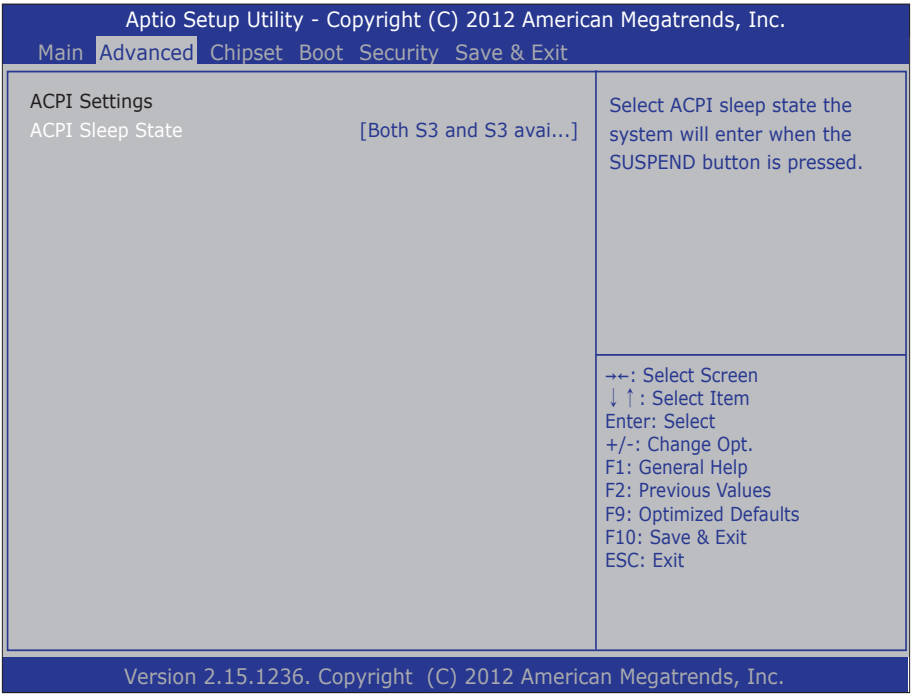


The featured submenus are:

Submenu	Description
ACPI Settings	See 3.2.1. ACPI Settings on page 37.
CPU Configuration	See 3.2.2. CPU Configuration page 38.
SATA Configuration	See 3.2.3. SATA Configuration on page 39.
AMT Configuration	See 3.2.4. AMT Configuration on page 42.
USB Configuration	See 3.2.5. USB Configuration on page 44.
Super IO Configuration	See 3.2.6. F71869E Super IO Configuration on page 46.
H/W Monitor	See 3.2.7. H/W Monitor on page 48.
Serial Port Console Redirection	See 3.2.8. Serial Port Console Redirection on page49
Intel® Ethernet Network Connection I217-LM	See 3.2.9. Intel Ethernet Network Connection i217-LH on page 51
Intel® I210 Gigabit Network Connection	See 3.2.10. Intel I210 Gigabit Network Connection on page 52

3.2.1. ACPI Settings

Access this submenu to configure the system's ACPI (Advanced Configuration and Power Interface).

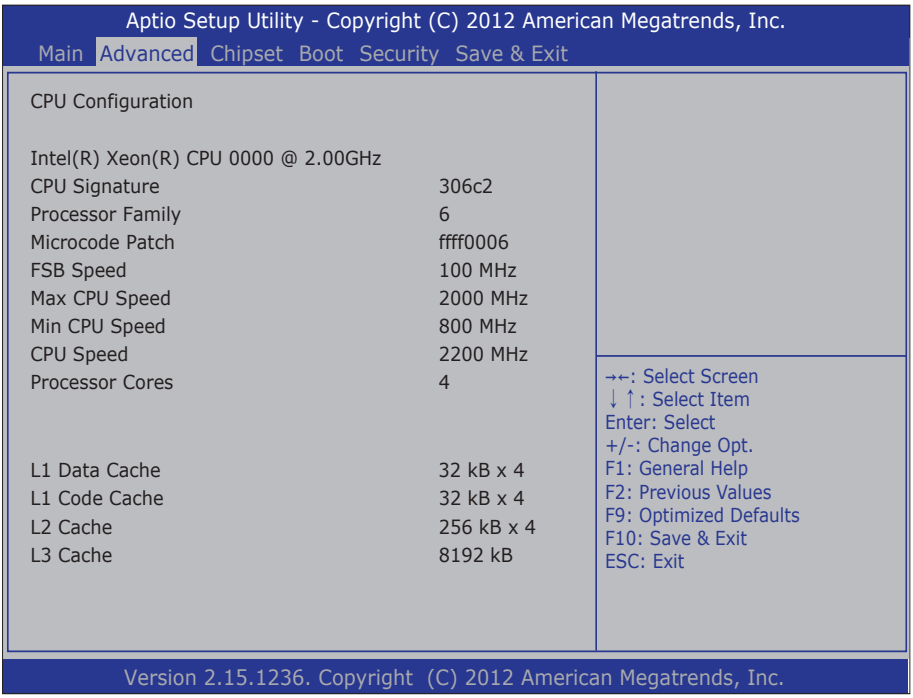


The featured submenus are:

Setting	Description
ACPI Sleep State	Sets the highest ACPI sleep state that system enters when the suspend button is hit. ▸ Options available are: ▸ **Suspend Disabled** ▸ **S1** only **(CPU Stop Clock)** ▸ **S3** only **(Suspend to RAM)** ▸ **Both S1** and **S3 available for OS choose from**

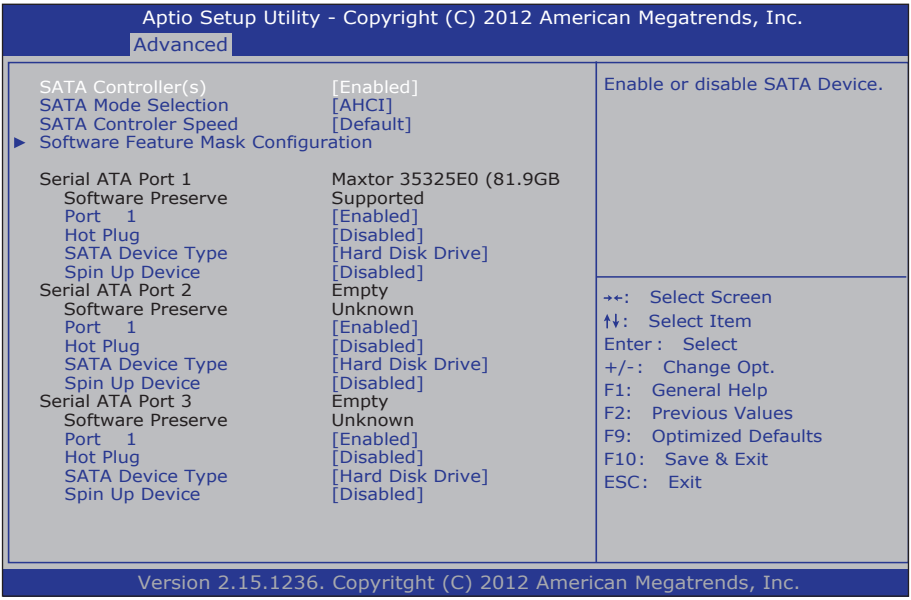
3.2.2. CPU Configuration

Access this submenu to identify the CPU and its capabilities by running a report listing the CPU's model name, processor speed, microcode revision, max./min. processor speeds, processor cores, and so on.



3.2.3. SATA Configuration

Access this submenu to view SATA device(s) information and also to configure SATA device(s).



The featured settings are:

Setting	Description
SATA Controller(s)	Enables/disables SATA device(s). ▸ **Enabled** is the default.
SATA Mode Selection	Configures how SATA controller(s) operate. ▸ Options available are **IDE** (default), **AHCI** and **RAID**.
SATA Controller Speed	Sets the maximum speed for the SATA controller to support. ▸ Options available are: **Default**, **Gen1**, **Gen2** and **Gen3**. ▸ This setting is available only when **SATA Mode Selection** is set to **AHCI** or **RAID**.

Software Feature Mask Configuration

This is a submenu to configure the features of RAID (Redundant Array of Inexpensive Disks).The featured settings are:

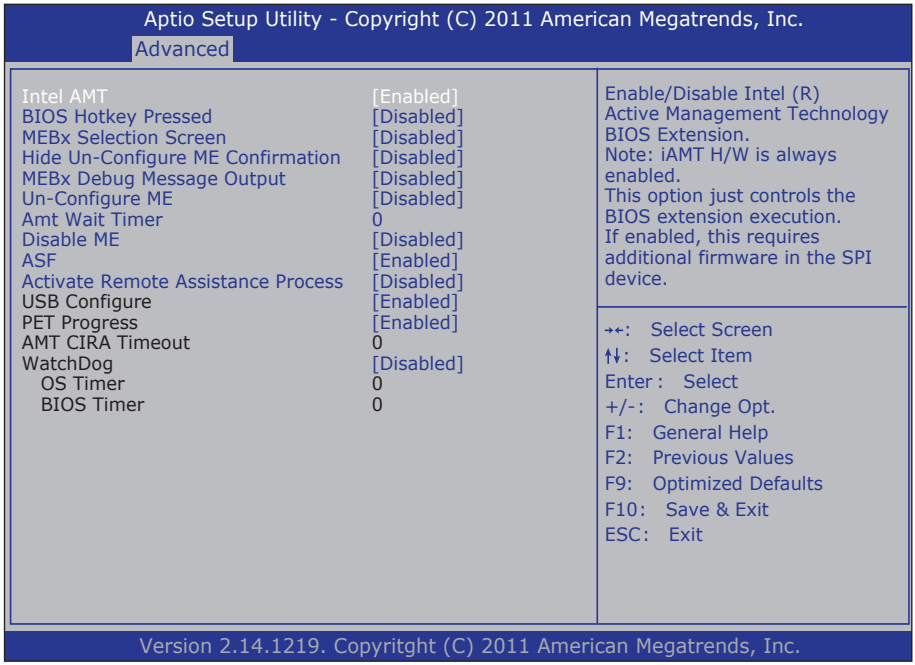
Setting	Description
RAID0	Enables/disables RAID0. ▸ **Enabled** is the default.
RAID1	Enables/disables RAID1. ▸ **Enabled** is the default.
RAID10	Enables/disables RAID10. ▸ **Enabled** is the default.
RAID5	Enables/disables RAID5. ▸ **Enabled** is the default.
Intel Rapid Recovery Technology	Enables/Disables Intel Rapid Recovery Technology. ▸ **Enabled** is the default.
OROM UI and BANNER	If enabled, then the OROM UI is shown, otherwise no OROM banner or information will be displayed if all disks and RAID volumes are Normal. ▸ Default is “Enabled”
HDD Unlock	If enabled, indicates that the HDD password unlock in the OS is enabled. ▸ Default is “Enabled”
LED Locate	If enabled, indicates that the LED/SGPIO hardware is attached and ping to locate feature is enabled on the OS. ▸ Default is “Enabled”
IRRT Only on eSATA	If enabled, then only IRRT volumes can span internal and eSATA drives. If disabled, then any RAID volume can span internal and eSATA drives.
Smart Response Tehcnology	Enables/Disables Smart Response Technology. ▸ Default is “Enabled”
OROM UI Delay	If enabled, indicates the delay of the OROM UI Splash screen in a normal status. ▸ Default is “2 Seconds”

▸ This submenu is available only when **SATA Mode Selection** is set to **AHCI** or **RAID**.

<table>
<tr><td rowspan="2">Serial ATA Port 1/2/3/4/5/6</td><td>Features the following settings:
<table>
<tr><th>Setting</th><th>Description</th></tr>
<tr><td>Port 1/2/3/4/5/6</td><td>Enables/disables the SATA port.
▸ Enabled is the default.</td></tr>
<tr><td>Hot Plug</td><td>Sets whether to make the SATA port an hot pluggable one.
▸ Disabled is the default.</td></tr>
<tr><td>External SATA</td><td>Enables/disables external SATA support.
▸ Disabled is the default.</td></tr>
<tr><td>SATA Device Type</td><td>Defines whether the SATA port is connected to a Solid State Drive or Hard Disk Drive.
▸ Hard Disk Drive is the default.</td></tr>
<tr><td>Spin Up Device</td><td>For the platforms with numerous Serial ATA hard disk drives, the power issue regarding the electrical current load during system power-up is often critical. This setting enables/disables “Staggered Spin Up”, which provides a simple mechanism for SATA HBAs (host bus adapters) to sequence disk drive initialization and spin-up.
▸ Disabled is the default.</td></tr>
</table></td></tr>
<tr><td>▸ These settings are available only when SATA Mode Selection is set to AHCI or RAID.</td></tr>
</table>

3.2.4. AMT Configuration

Intel® Active Management Technology (Intel® AMT) is a hardware-based solution that uses out-of-band communication for basic management of client systems, which allows a system administrator to monitor and manage the computers and other network equipment by remote control even if the hard drive is crashed, the system is turned off or the operating system is locked.



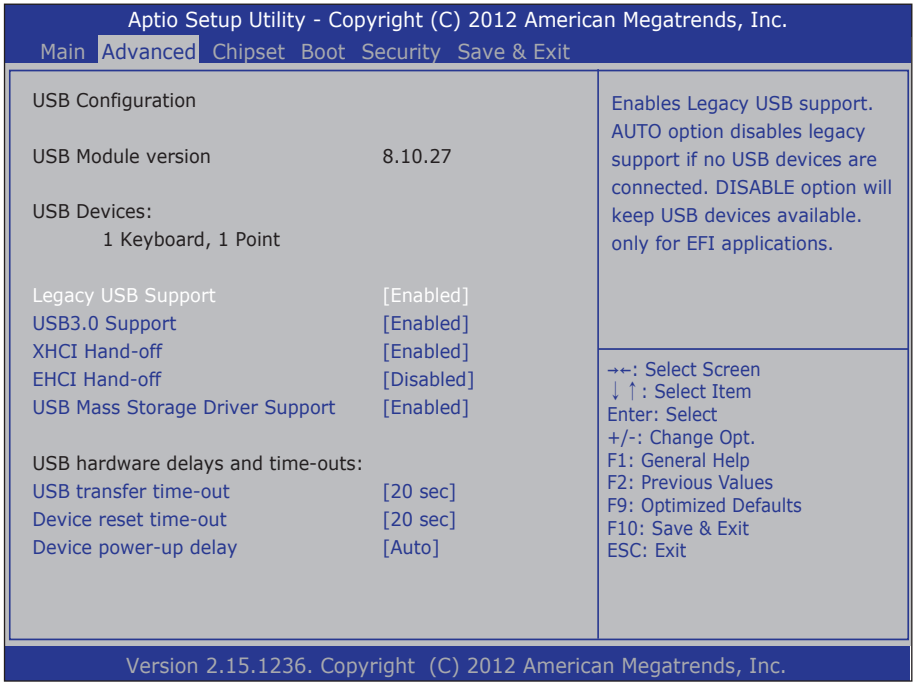
The featured settings are:

Setting	Description
Intel AMT	Enables/disables Intel® Active Management Technology BIOS extensions. ▸ **Enabled** is the default. **Note**. iAMT hardware is always enabled. This setting only controls BIOS extension execution. When enabled, additional firmware is required in the SPI device.
BIOS Hotkey Pressed	Enables/disables BIOS Hotkey Press function ▸ **Disabled** is the default.

<table>
<tr><td>MEBx Selection Screen</td><td>Enables/disables MEBx Selection Screen function.
▸ Disabled is the default.</td></tr>
<tr><td>Hide Un-Configure ME Confirmation</td><td>Enables/disables Hide Un-Configure ME without password Configuration Prompt function.
▸ Disabled is the default.</td></tr>
<tr><td>MEBx Debug Message Output</td><td>Enables/disables MEBx Debug Message Output function.
▸ Disabled is the default.</td></tr>
<tr><td>Un-Configure ME</td><td>Enables/disables Un-Configure ME without password function.
▸ Disabled is the default.</td></tr>
<tr><td>Amt Wait Timer</td><td>Set time to wait before sending ASF_GET_BOOT_OPTIONS.</td></tr>
<tr><td>Disable ME</td><td>Set ME to soft Temporary Disabled function</td></tr>
<tr><td>ASF</td><td>Enables/disables Alert Specification Format, a DMTF (Distributed Management Task Force) standard for remote monitoring, management and control of computer system in both OS-present and OS-absent environments.
▸ Enabled is the default.</td></tr>
<tr><td>Activate Remote Assistance Process</td><td>Enables/disables CIRA (Client-Initiated Remote Access) boot.
▸ Disabled is the default.</td></tr>
<tr><td>USB Configure</td><td>Enables/disables USB Configure function.
▸ Disabled is the default.</td></tr>
<tr><td>PET Progress</td><td>Enables/disables PET events progress to receive PET event or not.</td></tr>
<tr><td>AMT CIRA Timeout</td><td>Customizes the time-out for the establishment of MPS connection.
▸ This setting is only available when Activate Remote Assistance Process is enabled.
▸ Set it to 0 to use the default time-out value of 60 seconds.
▸ Set it to 255 to have MEBx wait until the connection succeeds.
▸ CIRA means “Client Initiated Remote Access”.</td></tr>
<tr><td>WatchDog</td><td>Enables/disables WatchDog Timer. When set as [Enabled], the following sub-items will be available.
<table>
<tr><th>Setting</th><th>Description</th></tr>
<tr><td>OS Timer</td><td>Set OS watch dog timer.</td></tr>
<tr><td>BIOS Timer</td><td>Set BIOS watch dog timer.</td></tr>
</table>
</td></tr>
</table>

3.2.5. USB Configuration

Access this submenu to view the USB device(s) enabled in the system. It also configures USB-related features.



The featured settings are:

Setting	Description / Available Options
Legacy USB Support	Enables/disables legacy USB support including USB flash drives and USB hard drives. Options available are ▸ **Enabled**: To enable legacy USB support. ▸ **Disabled**: To keep USB devices available only for EFI specification, ▸ **Auto**: To disable legacy support if no USB devices are connected.
USB3.0 Support	Enables/disables USB 3.0 controller support. ▸ **Enabled** is the default.
XHCI Hand-off	This is a workaround for OSes without XHCI hand-off support. The XHCI ownership change should be claimed by XHCI driver. The optional settings are: **Enabled / Disabled**.

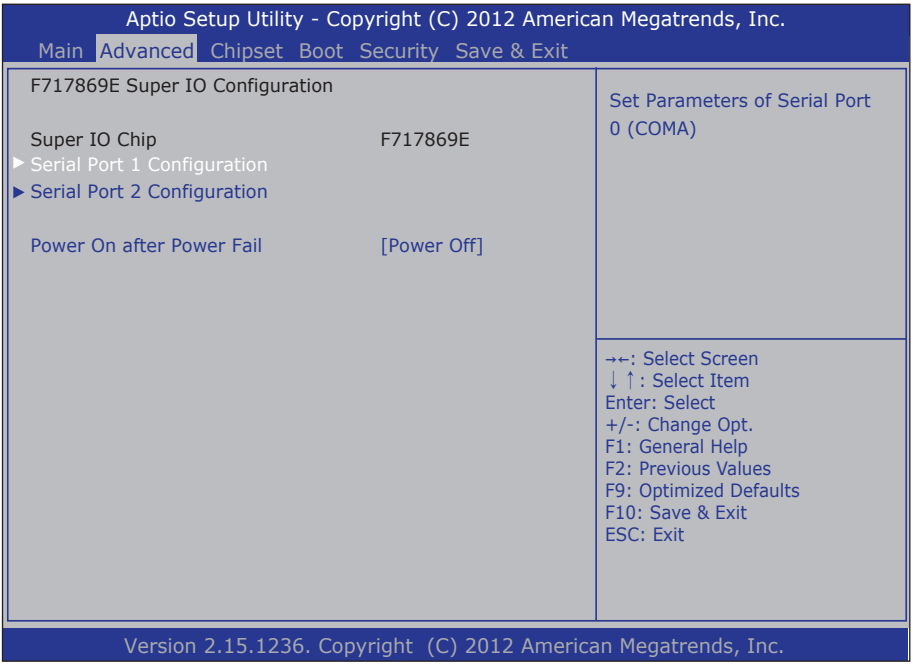
<table>
<tr><td>EHCI Hand-off</td><td>This is a workaround for OSes without EHCI hand-off support. The EHCI ownership change should be claimed by EHCI driver.
The optional settings are: Disabled / Enabled.</td></tr>
<tr><td>USB Mass Storage Driver Support</td><td>Enables/disables USB Mass Storage Driver Support.
The optional settings are: Disabled / Enabled.</td></tr>
<tr><td>USB hardware delay and time-out</td><td>This is a submenu to configure the features of USB hardware delay and time-out. The featured settings are:

<table>
<tr><th>Setting</th><th>Description</th></tr>
<tr><td>USB Transfer time-out</td><td>Use this item to set the time-out value for control, bulk, and interrupt transfers.
▸ Options available are: 1 sec, 5 sec, 10 sec, 20 sec</td></tr>
<tr><td>Device reset time-out</td><td>Use this item to set USB mass storage device start unit command time-out.
▸ Options available are: 10 sec, 20 sec, 30 sec, 40 sec</td></tr>
<tr><td>Device power-up delay</td><td>Use this item to set maximum time the device will take before it properly reports itself to the host controller. ‘Auto’ uses default value: for a root port it is 100 ms, for a hub port the delay is taken from hub descriptor.

▸ Options available are:
Auto: Default
Manual: Select Manual you can set value for the following sub-item: ‘Device Power-up delay in seconds’, the delay range in from 1 to 40 seconds, in one second increments.</td></tr>
</table>
</td></tr>
</table>

3.2.6. F71869E Super IO Configuration

This submenu opens in context with the system's serial ports, COM1 and COM2, to configure the Super IO chipset.



The featured settings are:

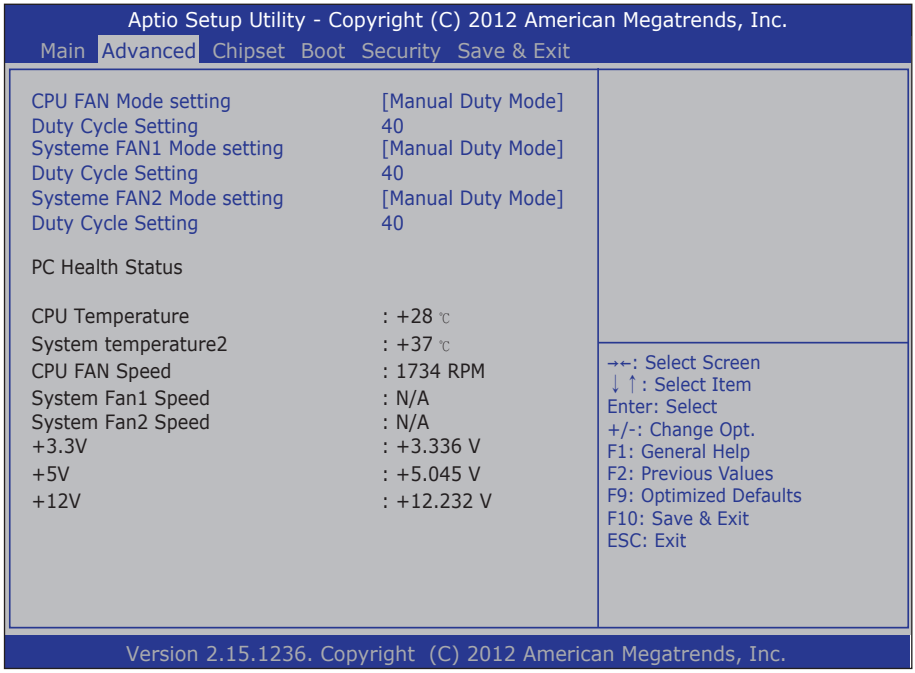
Submenu/Setting	Description
Serial Port 1 Configuration	Configures the system's serial port (COM port). The featured settings are:

Setting	Description
Serial Port	Enables/disables the serial port. ▸ **Enabled** is the default.
Serial Port 1 Interface	▸ Options available are: **RS422** /**RS232** / **RS485**
Change Settings	Sets the optimal IO address and IRQ info for the serial port. ▸ Options available are: **IO=3F8h; IRQ=4** (default) **IO=3F8h; IRQ=3,4,5,6,7,9,10,11,12**; **IO=2F8h; IRQ=3,4,5,6,7,9,10,11,12**; **IO=3E8h; IRQ=3,4,5,6,7,9,10,11,12**; **IO=2E8h; IRQ=3,4,5,6,7,9,10,11,12**;

<table>
<tr><td>Serial Port 2 Configuration</td><td>Configures the system's serial port (COM port). The featured settings are:
<table>
<tr><th>Setting</th><th>Description</th></tr>
<tr><td>Serial Port</td><td>Enables/disables the serial port.
▸ Enabled is the default.</td></tr>
<tr><td>Serial Port 2 interface</td><td>▸ Options available are: RS422 /RS232 / RS485</td></tr>
<tr><td>Change Settings</td><td>Sets the optimal IO address and IRQ info for the serial port.
▸ Options available are:
IO=2F8h; IRQ=3 (default)
IO=3F8h; IRQ=3,4,5,6,7,9,10,11,12;
IO=2F8h; IRQ=3,4,5,6,7,9,10,11,12;
IO=3E8h; IRQ=3,4,5,6,7,9,10,11,12;
IO=2E8h; IRQ=3,4,5,6,7,9,10,11,12;</td></tr>
</table></td></tr>
<tr><td>Power On After Power Fail</td><td>Set the power state after a power outage. Select Power Off for the system power to remain off after a power loss. Select Power On for the system power to be turned on after a power loss.
▸ Options available are: Power On / Power Off (Default)</td></tr>
</table>

3.2.7. H/W Monitor

Access this submenu to view the system's hardware health status and change system fan setting.

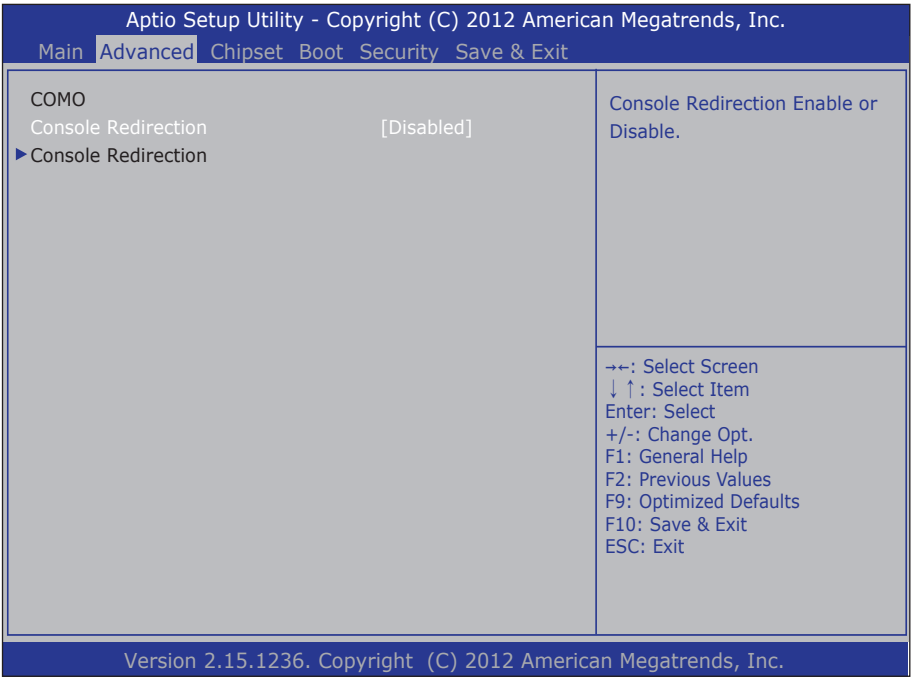


The featured settings are:

Setting	Description
CPU FAN/System FAN1/2 Mode setting	Set the Fan control mode ▸ Options available are: **Manual Duty Mode (Default)** **Auto Fan by CPU PWM Duty**
Manual Duty Mode	**Duty Cycle Setting**: Set the CPU/System Fan at fixed Duty-cycle. Minimum is 0% and Maximum is 100%
Auto Fan by CPU PWM Duty	Set the CPU/System FAN according to the CPU/System temperature. **CPU Temperature Limit of Highest**: the maximum limit of CPU. **CPU Temperature Limit of Lowest**: the minimum limit of CPU. **CPU Fan Highest Setting:** Set the CPU/System Fan Highest Duty-cycle **CPU Fan Second Setting:** Set the CPU/System Fan Second Duty-cycle **CPU Fan Lowest Setting:** Set the CPU/System Fan lowest Duty-cycle
PC Health Status	Display the main board's hardware status.

3.2.8. Serial Port Console Redirection

Access this submenu to control processor's power management.

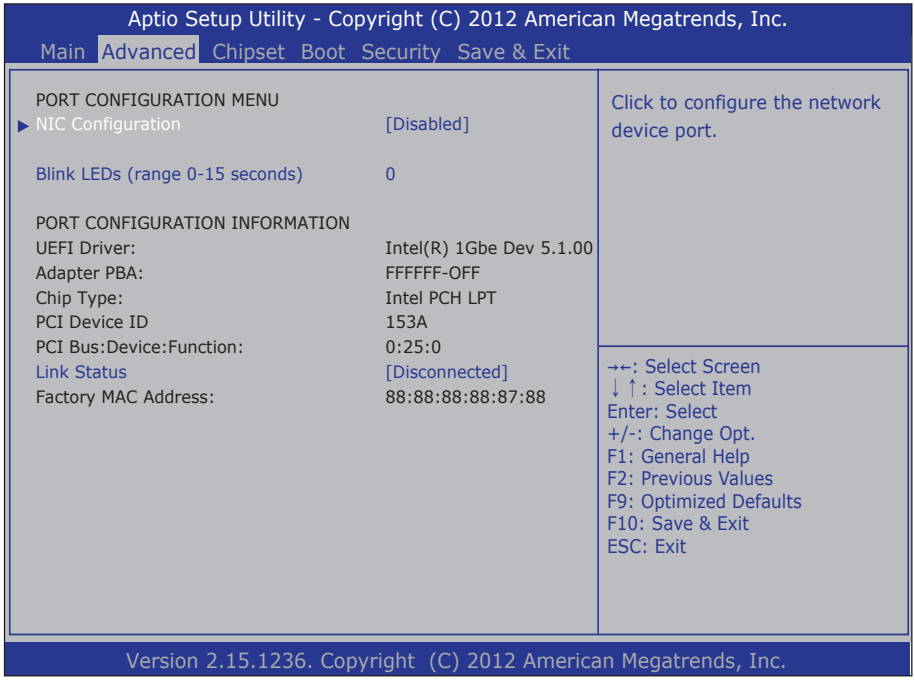


The featured settings are:

Setting		Description
Console Redirection		Enables/Disables console redirection ▸ **Disabled** is the default. ▸ Following submenu is available only when **Console Redirection** is set to **Enabled**.
Console Redirection	**Terminal Type**	Emulation: **ANSI:** Extended ASCII char set. **VT100:** ASCII char set. **VT100+:** Extends VT100 to support color, functional keys, etc. **VT-UTF8:** Uses UTF8 encoding to map unicode chars onto 1 or more bytes ▸ **ANSI** is the default.
	Bits per second	Selects serial port transmission speed. The speed must be matched on the other side. Long or noisy lines may require lower speeds. Default is "**115200**".

Console Redirection	**Data Bits**	Selects the Data Bits ▸ **8** is the default.
	Parity	A parity bit can be sent with the data bits to detect some transmission errors. **Even**: parity bit is 0 if the num of 1's in the data bits is even. **Odd**: parity bit is 0 if num of 1's in the data bits is odd. **Mark**: parity bit is always 1. **Space**: Parity bit is always 0. Mark and space parity do not allow for error detection. They can be used as an additional data bit. ▸ **None** is the default.
	Stop Bits	Stop bits indicate the end of a serial data packet. (A start bit indicates the beginning). The standard setting is 1 stop bit. Communication with slow devices may require more than 1 stop bit. ▸ **1** is the default.
	Flow Control	Flow control can prevent data loss from buffer overflow. When sending data, if the receiving buffers are full, a 'stop' signal can be sent to stop the data flow. Once the buffers are empty, a 'start' signal can be sent to restart the flow. Hardware flow control uses two wires to send start/stop signals. Software flow control uses start/stop ASCII chars, which slows down the data flow and can be problematic if binary data is being sent. ▸ **None** is the default.
	VT-UTF8 Combo Key support	Enables / Disables VT-UTF8 Combination Key Support for ANSI/ VT100 terminals. ▸ Options available are: **Disabled / Enabled**.
	Recorder mode	On this mode enabled only text will be send. This is to capture Terminal data. ▸ **Disabled** is the default.
	Resolution 100x31	Enables/Disables extended terminal resolution. ▸ **Disabled** is the default.
	Legacy OS Redirection	Stop bits indicate the end of a serial data packet. (A start bit indicates the beginning). The standard setting is 1 stop bit. Communication with slow devices may require more than 1 stop bit. ▸ **1** is the default.
	Putty KeyPad	Select F1~F12 function key setting on Putty ▸ Options available are: **VT100, LINUX, XTERMR6, SCO, ESCN, VT400**
	Redirection After BIOS POST	Set Redirection configuration after BIOS POST ▸ Options available are: **Always Enable**: set the Redirection to be always active **Boot Loader**: set the Redirection to be active during POST and Boot Loader

3.2.9. Intel Ethernet Network Connection i217-LH



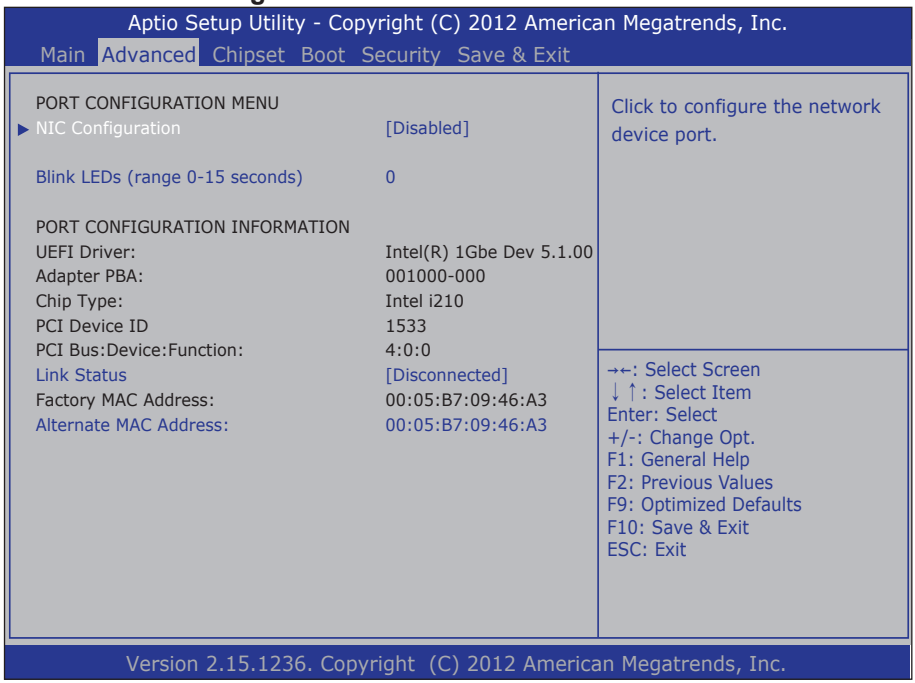
The featured settings are:

Setting	Description
NIC Configuration	Configure the Gigabit Ethernet device parameters of i217-LH

Setting	Description
Link Speed	Select the ethernet network speed ▸ **AutoNeg** is the default. ▸ Options are: **AutoNeg** **10Mbps Half** **10Mbps Full** **100Mbps Half** **100Mbps Full**
Wake on LAN	Enables/disables the Wake on LAN of Ethernet port ▸ **Enabled** is the default.

Blink LEDs	Configure the LED Blink speed (range from 0-15 seconds)
Link Status	Display the Link status

3.2.10. Intel I210 Gigabit Network Connection

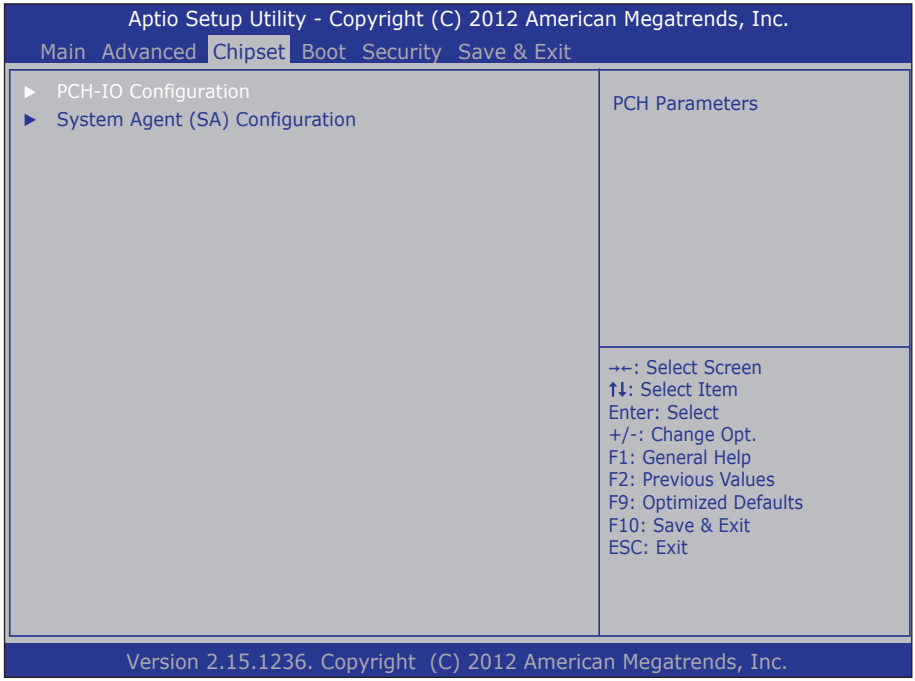


The featured settings are:

<table>
<tr><th>Setting</th><th>Description</th></tr>
<tr><td>NIC Configuration</td><td>Configure the Gigabit Ethernet device parameters of i210
<table>
<tr><th>Setting</th><th>Description</th></tr>
<tr><td>Link Speed</td><td>Select the Ethernet network speed
▸ AutoNeg is the default.
▸ Options are:
AutoNeg
10Mbps Half
10Mbps Full
100Mbps Half
100Mbps Full</td></tr>
<tr><td>Wake on LAN</td><td>Enables/disables the Wake on LAN of ethernet port
▸ Enabled is the default.</td></tr>
</table></td></tr>
<tr><td>Blink LEDs</td><td>Configure the LED Blink speed (range from 0-15 seconds).</td></tr>
<tr><td>Link Status</td><td>Display the Ethernet port link status.</td></tr>
<tr><td>Alternate MAC Address</td><td>Display the Alternate MAC Address of Ethernet port.</td></tr>
</table>

3.3. Chipset

Access this **Chipset** menu to configure the system's chipset.



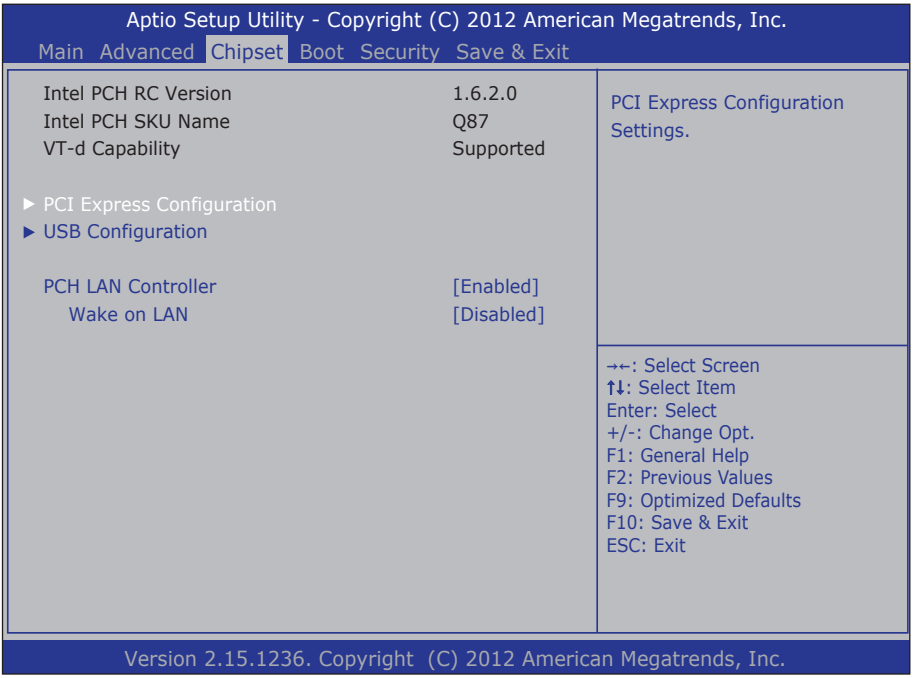
The featured submenu are **System Agent (SA) Configuration** and **PCH-IO Configuration**, which are covered in the following sections:

Submenu	Description
PCH-IO Configuration	Configures the PCH. ▸ See 3.3.1. PCH IO Configuration on page 54 for more details.
System Agent (SA) Configuration	Configures System Agent, i.e. the north bridge. ▸ See 3.3.2. System Agent (SA) Configuration on page 56 for more details.

WARNING: Wrong settings in these submenus may cause system malfunction.

3.3.1. PCH IO Configuration

Access this submenu to configure PCH parameters.



The featured settings are:

Setting/Submenu	Description
PCI Express Configuration	See 3.3.1.1. PCI Express Configuration on page 55.
USB Configuration	See 3.3.1.2. USB Configuration on page 55.
PC LAN Controller	Enables/disables the LAN port of PC ▸ Enabled is the default. **Wake on LAN :** Enables/disables the Wake on LAN of Ethernet ports.

3.3.1.1. PCI Express Configuration

Configures PCI Express by the following settings:

Setting	Description
PCI Express Root Port 1/2/3/4/5	▸ ASPM Support Options are: **Disable** : disables ASPM **L0s** : force all links to L0s state **L1** : force all links to L1 state **L0sL1** : force all links to L0s+L1 state **Auto** : BIOS auto configure ▸ PCIe Speed Options are: **Auto, Gen 1**, **Gen 2** **Auto** is the default.

3.3.1.2. USB Configuration

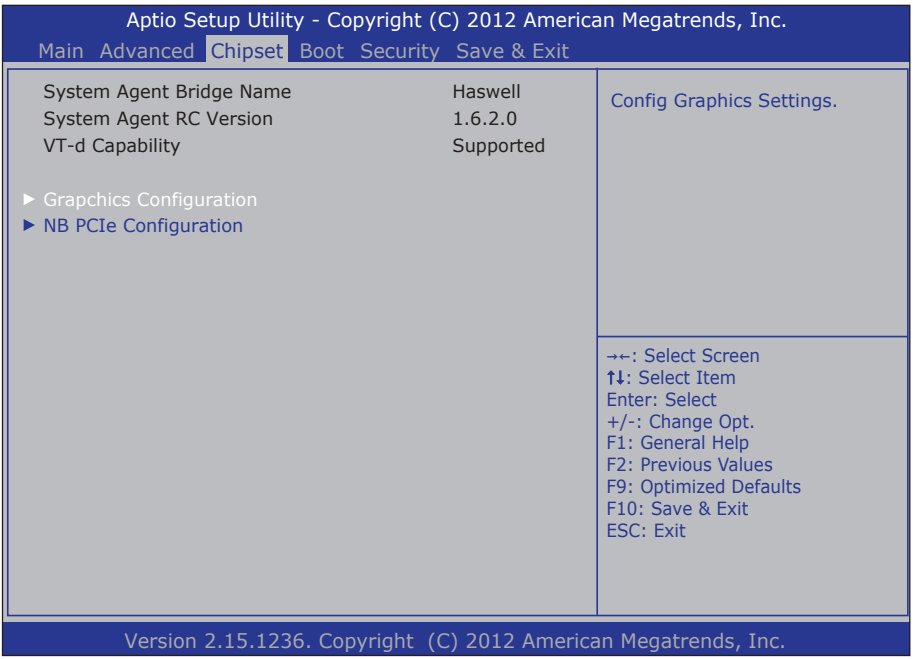
Access this submenu to configure the system's USB ports.

The featured settings are:

Setting	Description
USB Precondition	Precondition work on USB host controller and root ports for faster enumeration. ▸ Options available are: **Enabled/Disabled**. **Disabled** is the default.
xHCI Mode	Configures how the xHCI controller works. ▸ Select **Smart Auto** to have the BIOS avoid downgrading the USB 3.0 ports to 2.0 before the O.S. loads USB 3.0 driver. ▸ Select **Auto** to have the onboard USB 3.0 port function like 2.0 ports before the O.S. loads USB 3.0 driver, which is the default. ▸ Select **Enabled** to make the onboard USB 3.0 ports function like 3.0 ones. ▸ Select **Disabled** to make the onboard USB 3.0 ports function like 2.0 ones, which is optimal for the OS that does not have built-in USB 3.0 driver ▸ Select **Manual** to choose the mode manually.
BTCG	Allows you to enable or disable trunk clock gating ▸ Options available are: Enabled/Disabled
USB Ports Per-Port Disable Control	Respectively enables/disables a USB port. ▸ **Disabled** is the default.

3.3.2. System Agent (SA) Configuration

Access this submenu to configure the system agent.



The featured settings are:

Setting / Submenu	Description
Graphics Configuration	Configures the system's graphics. See 3.3.2.1. Graphics Configuration on page 57.
NB PCIe Configuration	See 3.3.2.3. NB PCIe Configuration on page 58.

3.3.2.1. Graphics Configuration

Select **Graphics Configuration** to view graphics info and accesses graphics settings.

The featured settings are:

Setting	Description
IGFX VBIOS Version	Display the IGFX(internal VGA) VBIOS version.
IGFX Frequency	Display the IGFX freqency
Graphics Turbo IMON Current	Sets the graphics turbo IMON current values. ▸ Options available are **14** to **31**. ▸ **31** is the default.
LCD Control	**Primary IGFX Boot Display** Select the video device which will be activated during POST. Note: This option won't be effective when external graphic is using. Secondary Boot display selection will appear based on your selection. VGA mode will be supported only on primary display. ▸ Options available are **VBIOS (Default)**, **CRT**, **Display Port**, **DVI**.

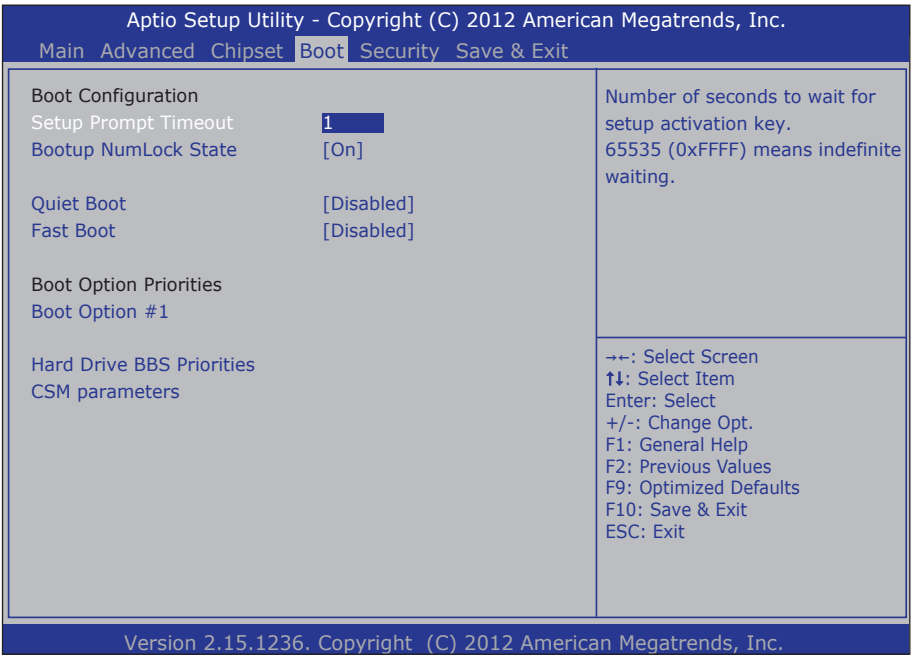
3.3.2.2. NB PCIe Configuration

Access this submenu to configure the system's PCIe.

Setting	Description
PEG0	Display the PEG0 status.
PEG0-Gen X	Configure the PEG0 ▸ Options available are Auto/Gen1/Gen2/Gen3. ▸ Auto is the default.
PEG1	Display the PEG1 status.
PEG1-Gen X	Configure the PEG1 ▸ Options available are Auto/Gen1/Gen2/Gen3. ▸ Auto is the default.
PEG2	Display the PEG2 status.
PEG2-Gen X	Configure the PEG2 ▸ Options available are Auto/Gen1/Gen2/Gen3. ▸ Auto is the default.
PEG1-ASPM	Configure ASPM support for the PEG Device. Note: This has no effect if PEG is not the currently active device. Options available are: **Disabled/Auto/ASPM L0s/ ASPM L1/APSM L0sL1**. **Auto** is the default.
PEG2-ASPM	Configure ASPM support for the PEG Device. Note: This has no effect if PEG is not the currently active device. Options available are: **Disabled/Auto/ASPM L0s/ ASPM L1/APSM L0sL1**. **Auto** is the default.

3.4. Boot

Access this menu to change system boot settings.



The featured submenu is:

Setting	Description
Setup Prompt Timeout	Sets how long to wait for the prompt for entering BIOS Setup to show. ▸ The default setting is **0** (sec). ▸ Set it to **65535** to wait indefinitely.
Bootup NumLock State	Sets whether to enable or disable the keyboard's NumLock state when the system starts up. ▸ Options available are **On** (default) and **Off**.
Quiet Boot	Sets whether to display the POST (Power-on Self Tests) messages or the system manufacturer's full screen logo during booting. ▸ Leave it as **Disabled**, which is the default, to display the normal POST message.

Fast Boot	Enables/disables initializing only a minimal set of devices required to launch the active boot options when booting up the system. ▸ **Disabled** is the default. ▸ This setting has no effect for BBS (BIOS Boot Specification) options. ▸ Options available are: **Enabled/Disabled**.
Hard Drive BBS Priorities	Sets the very 1st boot device among the available storage drives. ▸ BBS means “BIOS Boot Specification”.
CSM Parameters	Access this submenu to configure the execution of OpROM, boot options filter and so on. See the full settings at 3.4.1 CSM Parameters on page 61

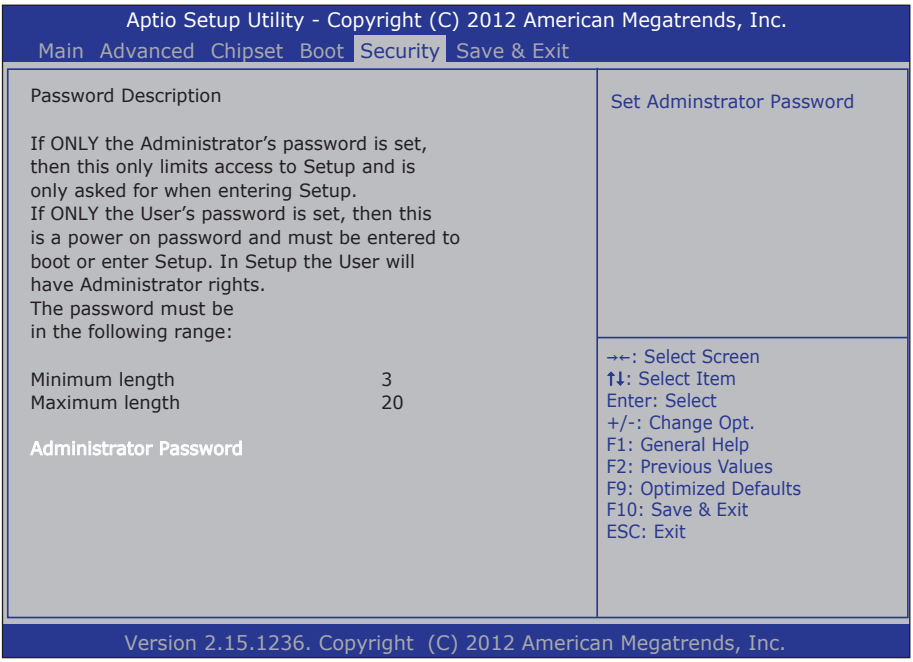
3.4.1 CSM Parameters

Access this submenu to configure the CSM parameters:

Setting	Description
Launch CSM	Enables/disables launching CSM (capability support module), which provides UEFI with the additional functionality to allow loading a traditional OS or using a traditional OpROM. ▸ Options available are: **Always** (default) and **Never**.
Boot Option Filter	Defines the devices to boot the system to. ▸ Options available are **UEFI and Legacy** (default), **Legacy only** and **UEFI only**. ▸ This setting is only available when **Launch CSM** is enabled (set to **Always**).
Launch PXE OpROM policy	Configures whether to launch the UEFI or legacy OpROM of PXE (Preboot eXecution Environment). ▸ Options available are **Do not launch** (default), **UEFI only** and **Legacy only**. ▸ This setting is only available when **Launch CSM** is enabled (set to **Always**).
Launch Storage OpROM policy	Configures whether to launch the UEFI or legacy OpROM of storage. ▸ Options available are **Do not launch**, **UEFI only** and **Legacy only** (default). ▸ This setting is only available when **Launch CSM** is enabled (set to **Always**).
Launch Video OpROM policy	Configures whether to launch the UEFI or legacy OpROM of video. ▸ Options available are **Do not launch**, **UEFI only** and **Legacy only** (default). ▸ This setting is only available when **Launch CSM** is enabled (set to **Always**).
Other PCI device ROM priority	Configures which OpROM to run for the PCI devices other than network, mass storage, or video. ▸ Options available are **UEFI OpROM** and **Legacy OpROM** (default).

3.5. Security

The **Security** menu sets up the administrator password. Once an administrator password is set up, this BIOS Setup utility is limited to access and will ask for the password each time any access is attempted.

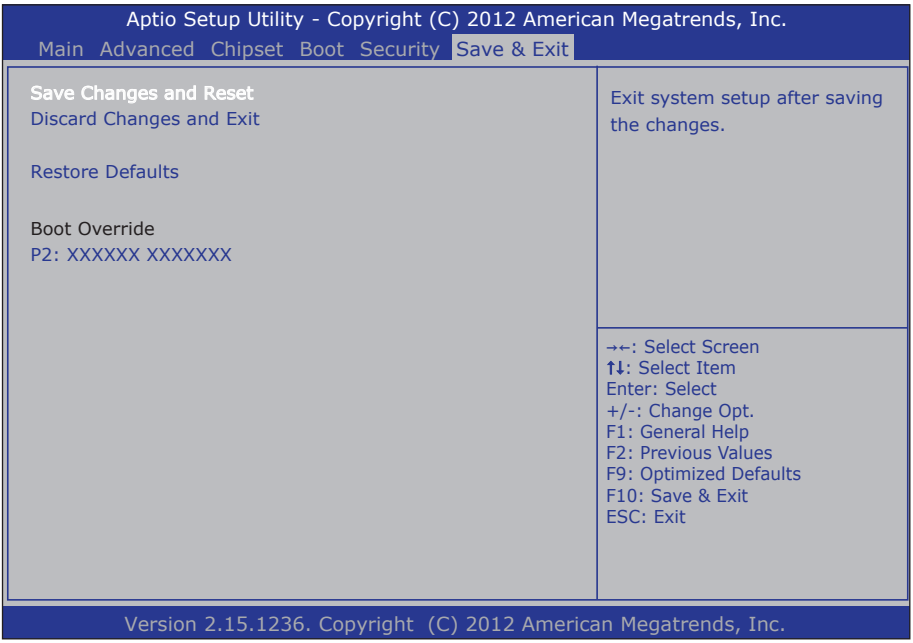


The featured settings are:

Setting	Description
Administrator Password	To set up an administrator password: 1. Select **Administrator Password**. A **Create New Password** dialog then pops up onscreen. 2. Enter your desired password that is no less than 3 characters and no more than 20 characters. 3. Hit [Enter] key to submit.

3.6. Save & Exit

The **Exit** menu features a handful of commands to launch actions from the BIOS Setup utility regarding saving changes, quitting the utility and recovering defaults.



The featured settings are:

Setting	Description
Save Changes and Exit	Saves the changes and quits the BIOS Setup utility. ▸ This is a command to launch an action from the BIOS Setup utility. ▸ When prompted for confirmation, select **OK** to save the changes and quit the BIOS Setup, or select **Cancel** to return to BIOS Setup.
Discard Changes and Exit	Discards the changes and quits the BIOS Setup utility. ▸ This is a command to launch an action from the BIOS Setup utility. ▸ When prompted for confirmation, select **OK** to quit BIOS Setup without saving the change(s), or select **Cancel** to return to the BIOS setup.
Restore Defaults	Loads the defaults to all settings. ▸ This is a command to launch an action from the BIOS Setup utility. ▸ When prompted for confirmation, select **OK** to load the defaults, or select **Cancel** to return to the BIOS setup.
Boot Override	**Boot Override** presents a list in context with the boot devices installed in the system. Select the device to boot up the system regardless of the currently configured boot priority. ▸ This is a command to launch action from the BIOS Setup utility.

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Appendices

Appendix A. AMI BIOS Checkpoints

A.1. Bootblock Initialization Code Checkpoints

The Bootblock initialization code sets up the chipset, memory and other components before system memory is available. The following table describes the type of checkpoints that may occur during the bootblock initialization portion of the BIOS (Note):

Checkpoint	Description
Before D0	If boot block debugger is enabled, CPU cache-as-RAM functionality is enabled at this point. Stack will be enabled from this point.
D0	Early Boot Strap Processor (BSP) initialization like microcode update, frequency and other CPU critical initialization. Early chipset initialization is done.
D1	Early super I/O initialization is done including RTC and keyboard controller. Serial port is enabled at this point if needed for debugging. NMI is disabled. Perform keyboard controller BAT test. Save power-on CPUID value in scratch CMOS. Go to flat mode with 4GB limit and GA20 enabled.
D2	Verify the boot block checksum. System will hang here if checksum is bad.
D3	Disable CACHE before memory detection. Execute full memory sizing module. If memory sizing module not executed, start memory refresh and do memory sizing in Boot block code. Do additional chipset initialization. Re-enable CACHE. Verify that flat mode is enabled.
D4	Test base 512KB memory. Adjust policies and cache first 8MB. Set stack.
D5	Bootblock code is copied from ROM to lower system memory and control is given to it. BIOS now executes out of RAM. Copies compressed boot block code to memory in right segments. Copies BIOS from ROM to RAM for faster access. Performs main BIOS checksum and updates recovery status accordingly.
D6	Both key sequence and OEM specific method is checked to determine if BIOS recovery is forced. If BIOS recovery is necessary, control flows to checkpoint E0. See Bootblock Recovery Code Checkpoints section of document for more information.
D7	Restore CPUID value back into register. The Bootblock-Runtime interface module is moved to system memory and control is given to it. Determine whether to execute serial flash.

Checkpoint	Description
D8	The Runtime module is uncompressed into memory. CPUID information is stored in memory.
D9	Store the Uncompressed pointer for future use in PMM. Copying Main BIOS into memory. Leaves all RAM below 1MB Read-Write including E000 and F000 shadow areas but closing SMRAM.
DA	Restore CPUID value back into register. Give control to BIOS POST (ExecutePOSTKernel). See POST Code Checkpoints section of document for more information.
DC	System is waking from ACPI S3 state
E1-E8 EC-EE	OEM memory detection/configuration error. This range is reserved for chipset vendors & system manufacturers. The error associated with this value may be different from one platform to the next.

A.2. Bootblock Recovery Code Checkpoints

The Bootblock recovery code gets control when the BIOS determines that a BIOS recovery needs to occur because the user has forced the update or the BIOS checksum is corrupt. The following table describes the type of checkpoints that may occur during the Bootblock recovery portion of the BIOS (Note):

Checkpoint	Description
E0	Initialize the floppy controller in the super I/O. Some interrupt vectors are initialized. DMA controller is initialized. 8259 interrupt controller is initialized. L1 cache is enabled.
E9	Set up floppy controller and data. Attempt to read from floppy.
EA	Enable ATAPI hardware. Attempt to read from ARMD and ATAPI CDROM.
EB	Disable ATAPI hardware. Jump back to checkpoint E9.
EF	Read error occurred on media. Jump back to checkpoint EB.
F0	Search for pre-defined recovery file name in root directory.
F1	Recovery file not found.
F2	Start reading FAT table and analyze FAT to find the clusters occupied by the recovery file.
F3	Start reading the recovery file cluster by cluster.
F5	Disable L1 cache.
FA	Check the validity of the recovery file configuration to the current configuration of the flash part.
FB	Make flash write enabled through chipset and OEM specific method. Detect proper flash part. Verify that the found flash part size equals the recovery file size.
F4	The recovery file size does not equal the found flash part size.
FC	Erase the flash part.
FD	Program the flash part.
FF	The flash has been updated successfully. Make flash write disabled. Disable ATAPI hardware. Restore CPUID value back into register. Give control to F000 ROM at F000:FFF0h.

A.3. POST Code Checkpoints

The POST code checkpoints are the largest set of checkpoints during the BIOS pre-boot process. The following table describes the type of checkpoints that may occur during the POST portion of the BIOS (Note):

Checkpoint	Description
03	Disable NMI, Parity, video for EGA, and DMA controllers. Initialize BIOS, POST, Runtime data area. Also initialize BIOS modules on POST entry and GPNV area. Initialized CMOS as mentioned in the Kernel Variable "wCMOSFlags."
04	Check CMOS diagnostic byte to determine if battery power is OK and CMOS checksum is OK. Verify CMOS checksum manually by reading storage area. If the CMOS checksum is bad, update CMOS with power-on default values and clear passwords. Initialize status register A. Initializes data variables that are based on CMOS setup questions. Initializes both the 8259 compatible PICs in the system
05	Initializes the interrupt controlling hardware (generally PIC) and interrupt vector table.
06	Do R/W test to CH-2 count reg. Initialize CH-0 as system timer.Install the POSTINT1Ch handler. Enable IRQ-0 in PIC for system timer interrupt. Traps INT1Ch vector to "POSTINT1ChHandlerBlock."
07	Fixes CPU POST interface calling pointer.
08	Initializes the CPU. The BAT test is being done on KBC. Program the keyboard controller command byte is being done after Auto detection of KB/MS using AMI KB-5.
C0	Early CPU Init Start -- Disable Cache – Init Local APIC
C1	Set up boot strap processor Information
C2	Set up boot strap processor for POST
C5	Enumerate and set up application processors
C6	Re-enable cache for boot strap processor
C7	Early CPU Init Exit
0A	Initializes the 8042 compatible Key Board Controller.
0B	Detects the presence of PS/2 mouse.
0C	Detects the presence of Keyboard in KBC port.

Checkpoint	Description
0E	Testing and initialization of different Input Devices. Also, update the Kernel Variables. Traps the INT09h vector, so that the POST INT09h handler gets control for IRQ1. Uncompress all available language, BIOS logo, and Silent logo modules.
13	Early POST initialization of chipset registers.
20	Relocate System Management Interrupt vector for all CPU in the system.
24	Uncompress and initialize any platform specific BIOS modules. GPNV is initialized at this checkpoint.
2A	Initializes different devices through DIM. See DIM Code Checkpoints section of document for more information.
2C	Initializes different devices. Detects and initializes the video adapter installed in the system that have optional ROMs.
2E	Initializes all the output devices.
31	Allocate memory for ADM module and uncompress it. Give control to ADM module for initialization. Initialize language and font modules for ADM. Activate ADM module.
33	Initializes the silent boot module. Set the window for displaying text information.
37	Displaying sign-on message, CPU information, setup key message, and any OEM specific information.
38	Initializes different devices through DIM. See DIM Code Checkpoints section of document for more information. USB controllers are initialized at this point.
39	Initializes DMAC-1 & DMAC-2.
3A	Initialize RTC date/time.
3B	Test for total memory installed in the system. Also, Check for DEL or ESC keys to limit memory test. Display total memory in the system.
3C	Mid POST initialization of chipset registers.
40	Detect different devices (Parallel ports, serial ports, and coprocessor in CPU, … etc.) successfully installed in the system and update the BDA, EBDA…etc.
52	Updates CMOS memory size from memory found in memory test. Allocates memory for Extended BIOS Data Area from base memory. Programming the memory hole or any kind of implementation that needs an adjustment in system RAM size if needed.
60	Initializes NUM-LOCK status and programs the KBD typematic rate.

Checkpoint	Description
75	Initialize Int-13 and prepare for IPL detection.
78	Initializes IPL devices controlled by BIOS and option ROMs.
7C	Generate and write contents of ESCD in NVRam.
84	Log errors encountered during POST.
85	Display errors to the user and gets the user response for error.
87	Execute BIOS setup if needed / requested. Check boot password if installed.
8C	Late POST initialization of chipset registers.
8D	Build ACPI tables (if ACPI is supported)
8E	Program the peripheral parameters. Enable/Disable NMI as selected
90	Initialization of system management interrupt by invoking all handlers. Please note this checkpoint comes right after checkpoint 20h
A1	Clean-up work needed before booting to OS.
A2	Takes care of runtime image preparation for different BIOS modules. Fill the free area in F000h segment with 0FFh. Initializes the Microsoft IRQ Routing Table. Prepares the runtime language module. Disables the system configuration display if needed.
A4	Initialize runtime language module. Display boot option popup menu.
A7	Displays the system configuration screen if enabled. Initialize the CPU's before boot, which includes the programming of the MTRR's.
A9	Wait for user input at config display if needed.
AA	Uninstall POST INT1Ch vector and INT09h vector.
AB	Prepare BBS for Int 19 boot. Init MP tables.
AC	End of POST initialization of chipset registers. De-initializes the ADM module.
B1	Save system context for ACPI. Prepare CPU for OS boot including final MTRR values.
00	Passes control to OS Loader (typically INT19h).

A.4. DIM Code Checkpoints

The Device Initialization Manager (DIM) gets control at various times during BIOS POST to initialize different system busses. The following table describes the main checkpoints where the DIM module is accessed (Note):

Checkpoint	Description
2A	Initialize different buses and perform the following functions: Reset, Detect, and Disable (function 0); Static Device Initialization (function 1); Boot Output Device Initialization (function 2). Function 0 disables all device nodes, PCI devices, and PnP ISA cards. It also assigns PCI bus numbers. Function 1 initializes all static devices that include manual configured onboard peripherals, memory and I/O decode windows in PCI-PCI bridges, and noncompliant PCI devices. Static resources are also reserved. Function 2 searches for and initializes any PnP, PCI, or AGP video devices.
38	Initialize different buses and perform the following functions: Boot Input Device Initialization (function 3); IPL Device Initialization (function 4); General Device Initialization (function 5). Function 3 searches for and configures PCI input devices and detects if system has standard keyboard controller. Function 4 searches for and configures all PnP and PCI boot devices. Function 5 configures all onboard peripherals that are set to an automatic configuration and configures all remaining PnP and PCI devices.

While control is in the different functions, additional checkpoints are output to port 80h as a word value to identify the routines under execution. The low byte value indicates the main POST Code Checkpoint. The high byte is divided into two nibbles and contains two fields. The details of the high byte of these checkpoints are as follows:
HIGH BYTE XY
XY The upper nibble 'X' indicates the function number that is being executed. 'X' can be from 0 to 7.
0 = func#0, disable all devices on the BUS concerned.
1 = func#1, static devices initialization on the BUS concerned.
2 = func#2, output device initialization on the BUS concerned.
3 = func#3, input device initialization on the BUS concerned.
4 = func#4, IPL device initialization on the BUS concerned.
5 = func#5, general device initialization on the BUS concerned.
6 = func#6, error reporting for the BUS concerned.
7 = func#7, add-on ROM initialization for all BUSes.
8 = func#8, BBS ROM initialization for all BUSes.
The lower nibble 'Y' indicates the BUS on which the different routines are being

executed. 'Y' can be from 0 to 5.
0 = Generic DIM (Device Initialization Manager).
1 = On-board System devices.
2 = ISA devices.
3 = EISA devices.
4 = ISA PnP devices.
5 = PCI devices.

A.5. ACPI Runtime Checkpoints

ACPI checkpoints are displayed when an ACPI capable operating system either enters or leaves a sleep state. The following table describes the type of checkpoints that may occur during ACPI sleep or wake events (Note):

Checkpoint	Description
AC	First ASL check point. Indicates the system is running in ACPI mode.
AA	System is running in APIC mode.
01, 02, 03, 04, 05	Entering sleep state S1, S2, S3, S4, or S5.
10, 20, 30, 40, 50	Waking from sleep state S1, S2, S3, S4, or S5.

Note:
Please note that checkpoints may differ between different platforms based on system configuration. Checkpoints may change due to vendor requirements, system chipset or option ROMs from add-in PCI devices.

Appendix B. I/O Port Address Map

Each peripheral device in the system is assigned a set of I/O port addresses which also becomes the identity of the device.
The following table lists the I/O port addresses used.

Address	Device Description
0x000002F8-0x000002FF	Communications Port (COM2)
0x000003F8-0x000003FF	Communications Port (COM1)
0x00000040-0x00000043	System timer
0x00000050-0x00000053	System timer
0x00000070-0x00000077	System CMOS/real time clock
0x00000060-0x00000060	Standard PS/2 Keyboard
0x00000064-0x00000064	Standard PS/2 Keyboard
0x000004D0-0x000004D1	Programmable interrupt controller
0x00000020-0x00000021	Programmable interrupt controller
0x00000024-0x00000025	Programmable interrupt controller
0x00000028-0x00000029	Programmable interrupt controller
0x0000002C-0x0000002D	Programmable interrupt controller
0x00000030-0x00000031	Programmable interrupt controller
0x00000034-0x00000035	Programmable interrupt controller
0x00000038-0x00000039	Programmable interrupt controller
0x0000003C-0x0000003D	Programmable interrupt controller
0x000000A0-0x000000A1	Programmable interrupt controller
0x000000A4-0x000000A5	Programmable interrupt controller
0x000000A8-0x000000A9	Programmable interrupt controller
0x000000AC-0x000000AD	Programmable interrupt controller
0x000000B0-0x000000B1	Programmable interrupt controller
0x000000B4-0x000000B5	Programmable interrupt controller
0x000000B8-0x000000B9	Programmable interrupt controller
0x000000BC-0x000000BD	Programmable interrupt controller
0x00000000-0x00000CF7	PCI Bus
0x00000D00-0x0000FFFF	PCI Bus
0x000000F0-0x000000F0	Numeric data processor
0x00000070-0x00000077	Motherboard resources

Address	Device Description
0x00000010-0x0000001F	Motherboard resources
0x00000022-0x0000003F	Motherboard resources
0x00000044-0x0000005F	Motherboard resources
0x00000062-0x00000063	Motherboard resources
0x00000065-0x0000006F	Motherboard resources
0x00000065-0x0000006F	Motherboard resources
0x00000072-0x0000007F	Motherboard resources
0x00000080-0x00000080	Motherboard resources
0x00000080-0x00000080	Motherboard resources
0x00000084-0x00000086	Motherboard resources
0x00000088-0x00000088	Motherboard resources
0x0000008C-0x0000008E	Motherboard resources
0x00000090-0x0000009F	Motherboard resources
0x000000A2-0x000000BF	Motherboard resources
0x000000E0-0x000000EF	Motherboard resources
0x000004D0-0x000004D1	Motherboard resources
0x00000A00-0x00000A1F	Motherboard resources
0x00000290-0x000002AF	Motherboard resources
0x0000002E-0x0000002F	Motherboard resources
0x0000004E-0x0000004F	Motherboard resources
0x00000061-0x00000061	Motherboard resources
0x00000063-0x00000063	Motherboard resources
0x00000067-0x00000067	Motherboard resources
0x00000092-0x00000092	Motherboard resources
0x000000B2-0x000000B3	Motherboard resources
0x00000680-0x0000069F	Motherboard resources
0x0000FFFF-0x0000FFFF	Motherboard resources
0x0000FFFF-0x0000FFFF	Motherboard resources
0x0000FFFF-0x0000FFFF	Motherboard resources
0x00001C00-0x00001CFE	Motherboard resources
0x00001D00-0x00001DFE	Motherboard resources
0x00001E00-0x00001EFE	Motherboard resources
0x00001F00-0x00001FFE	Motherboard resources

Address	Device Description
0x00001800-0x000018FE	Motherboard resources
0x0000164E-0x0000164F	Motherboard resources
0x00001854-0x00001857	Motherboard resources
0x0000F000-0x0000F03F	Intel(R) HD Graphics P4600/P4700
0x000003B0-0x000003BB	Intel(R) HD Graphics P4600/P4700
0x000003C0-0x000003DF	Intel(R) HD Graphics P4600/P4700
0x0000F040-0x0000F05F	Intel(R) 8 Series/C220 Series SMBus Controller - 8C22
0x0000F0D0-0x0000F0D7	Intel(R) 8 Series/C220 Series SATA AHCI Controller - 8C02
0x0000F0C0-0x0000F0C3	Intel(R) 8 Series/C220 Series SATA AHCI Controller - 8C02
0x0000F0B0-0x0000F0B7	Intel(R) 8 Series/C220 Series SATA AHCI Controller - 8C02
0x0000F0A0-0x0000F0A3	Intel(R) 8 Series/C220 Series SATA AHCI Controller - 8C02
0x0000F060-0x0000F07F	Intel(R) 8 Series/C220 Series SATA AHCI Controller - 8C02
0x0000E000-0x0000EFFF	Intel(R) 8 Series/C220 Series PCI Express Root Port #4 - 8C16
0x00000000-0x00000CF7	Direct memory access controller
0x00000081-0x00000091	Direct memory access controller
0x00000093-0x0000009F	Direct memory access controller
0x000000C0-0x000000DF	Direct memory access controller

Appendix C. Interrupt Request Lines (IRQ)

Peripheral devices use interrupt request lines to notify CPU for the service required. The following table shows the IRQ used by the devices on board.

Level	Function
IRQ 0	System timer
IRQ 1	Standard PS/2 Keyboard
IRQ 3	Communications Port (COM2)
IRQ 4	Communications Port (COM1)
IRQ 8	System CMOS/real time clock
IRQ 11	Intel(R) 8 Series/C220 Series SMBus Controller - 8C22
IRQ 12	Microsoft PS/2 Mouse
IRQ 13	Numeric data processor
IRQ 16	Intel(R) Management Engine Interface
IRQ 16	Intel(R) 8 Series/C220 Series USB Enhanced Host Controller #2 - 8C2D
IRQ 16	High Definition Audio Controller
IRQ 19	Intel(R) 8 Series/C220 Series SATA AHCI Controller - 8C02
IRQ 22	High Definition Audio Controller
IRQ 23	Intel(R) 8 Series/C220 Series USB Enhanced Host Controller #1 - 8C26
IRQ 81	Microsoft ACPI-Compliant System
IRQ 82	Microsoft ACPI-Compliant System
IRQ 83	Microsoft ACPI-Compliant System
IRQ 84	Microsoft ACPI-Compliant System
IRQ 85	Microsoft ACPI-Compliant System
IRQ 86	Microsoft ACPI-Compliant System
IRQ 87	Microsoft ACPI-Compliant System
IRQ 88	Microsoft ACPI-Compliant System
IRQ 89	Microsoft ACPI-Compliant System
IRQ 90	Microsoft ACPI-Compliant System
IRQ 91	Microsoft ACPI-Compliant System
IRQ 92	Microsoft ACPI-Compliant System
IRQ 93	Microsoft ACPI-Compliant System
IRQ 94	Microsoft ACPI-Compliant System

Level	Function
IRQ 95	Microsoft ACPI-Compliant System
IRQ 96	Microsoft ACPI-Compliant System
IRQ 97	Microsoft ACPI-Compliant System
IRQ 98	Microsoft ACPI-Compliant System
IRQ 99	Microsoft ACPI-Compliant System
IRQ 100	Microsoft ACPI-Compliant System
IRQ 101	Microsoft ACPI-Compliant System
IRQ 102	Microsoft ACPI-Compliant System
IRQ 103	Microsoft ACPI-Compliant System
IRQ 104	Microsoft ACPI-Compliant System
IRQ 105	Microsoft ACPI-Compliant System
IRQ 106	Microsoft ACPI-Compliant System
IRQ 107	Microsoft ACPI-Compliant System
IRQ 108	Microsoft ACPI-Compliant System
IRQ 109	Microsoft ACPI-Compliant System
IRQ 110	Microsoft ACPI-Compliant System
IRQ 111	Microsoft ACPI-Compliant System
IRQ 112	Microsoft ACPI-Compliant System
IRQ 113	Microsoft ACPI-Compliant System
IRQ 114	Microsoft ACPI-Compliant System
IRQ 115	Microsoft ACPI-Compliant System
IRQ 116	Microsoft ACPI-Compliant System
IRQ 117	Microsoft ACPI-Compliant System
IRQ 118	Microsoft ACPI-Compliant System
IRQ 119	Microsoft ACPI-Compliant System
IRQ 120	Microsoft ACPI-Compliant System
IRQ 121	Microsoft ACPI-Compliant System
IRQ 122	Microsoft ACPI-Compliant System
IRQ 123	Microsoft ACPI-Compliant System
IRQ 124	Microsoft ACPI-Compliant System
IRQ 125	Microsoft ACPI-Compliant System
IRQ 126	Microsoft ACPI-Compliant System
IRQ 127	Microsoft ACPI-Compliant System

Level	Function
IRQ 128	Microsoft ACPI-Compliant System
IRQ 129	Microsoft ACPI-Compliant System
IRQ 130	Microsoft ACPI-Compliant System
IRQ 131	Microsoft ACPI-Compliant System
IRQ 132	Microsoft ACPI-Compliant System
IRQ 133	Microsoft ACPI-Compliant System
IRQ 134	Microsoft ACPI-Compliant System
IRQ 135	Microsoft ACPI-Compliant System
IRQ 136	Microsoft ACPI-Compliant System
IRQ 137	Microsoft ACPI-Compliant System
IRQ 138	Microsoft ACPI-Compliant System
IRQ 139	Microsoft ACPI-Compliant System
IRQ 140	Microsoft ACPI-Compliant System
IRQ 141	Microsoft ACPI-Compliant System
IRQ 142	Microsoft ACPI-Compliant System
IRQ 143	Microsoft ACPI-Compliant System
IRQ 144	Microsoft ACPI-Compliant System
IRQ 145	Microsoft ACPI-Compliant System
IRQ 146	Microsoft ACPI-Compliant System
IRQ 147	Microsoft ACPI-Compliant System
IRQ 148	Microsoft ACPI-Compliant System
IRQ 149	Microsoft ACPI-Compliant System
IRQ 150	Microsoft ACPI-Compliant System
IRQ 151	Microsoft ACPI-Compliant System
IRQ 152	Microsoft ACPI-Compliant System
IRQ 153	Microsoft ACPI-Compliant System
IRQ 154	Microsoft ACPI-Compliant System
IRQ 155	Microsoft ACPI-Compliant System
IRQ 156	Microsoft ACPI-Compliant System
IRQ 157	Microsoft ACPI-Compliant System
IRQ 158	Microsoft ACPI-Compliant System
IRQ 159	Microsoft ACPI-Compliant System
IRQ 160	Microsoft ACPI-Compliant System

Level	Function
IRQ 161	Microsoft ACPI-Compliant System
IRQ 162	Microsoft ACPI-Compliant System
IRQ 163	Microsoft ACPI-Compliant System
IRQ 164	Microsoft ACPI-Compliant System
IRQ 165	Microsoft ACPI-Compliant System
IRQ 166	Microsoft ACPI-Compliant System
IRQ 167	Microsoft ACPI-Compliant System
IRQ 168	Microsoft ACPI-Compliant System
IRQ 169	Microsoft ACPI-Compliant System
IRQ 170	Microsoft ACPI-Compliant System
IRQ 171	Microsoft ACPI-Compliant System
IRQ 172	Microsoft ACPI-Compliant System
IRQ 173	Microsoft ACPI-Compliant System
IRQ 174	Microsoft ACPI-Compliant System
IRQ 175	Microsoft ACPI-Compliant System
IRQ 176	Microsoft ACPI-Compliant System
IRQ 177	Microsoft ACPI-Compliant System
IRQ 178	Microsoft ACPI-Compliant System
IRQ 179	Microsoft ACPI-Compliant System
IRQ 180	Microsoft ACPI-Compliant System
IRQ 181	Microsoft ACPI-Compliant System
IRQ 182	Microsoft ACPI-Compliant System
IRQ 183	Microsoft ACPI-Compliant System
IRQ 184	Microsoft ACPI-Compliant System
IRQ 185	Microsoft ACPI-Compliant System
IRQ 186	Microsoft ACPI-Compliant System
IRQ 187	Microsoft ACPI-Compliant System
IRQ 188	Microsoft ACPI-Compliant System
IRQ 189	Microsoft ACPI-Compliant System
IRQ 190	Microsoft ACPI-Compliant System
IRQ 4294967282	Intel(R) I210 Gigabit Network Connection
IRQ 4294967283	Intel(R) I210 Gigabit Network Connection
IRQ 4294967284	Intel(R) I210 Gigabit Network Connection
IRQ 4294967285	Intel(R) I210 Gigabit Network Connection

Level	Function
IRQ 4294967286	Intel(R) I210 Gigabit Network Connection
IRQ 4294967287	Intel(R) I210 Gigabit Network Connection
IRQ 4294967288	Intel(R) Ethernet Connection I217-LM
IRQ 4294967289	Intel(R) USB 3.0 Extensible Host Controller
IRQ 4294967290	**Intel(R) HD Graphics P4600/P4700**
IRQ 4294967291	**PCI standard PCI Express to PCI/PCI-X Bridge**
IRQ 4294967292	**Intel(R) 8 Series/C220 Series PCI Express Root Port #4 - 8C16**
IRQ 4294967293	**Intel(R) 8 Series/C220 Series PCI Express Root Port #2 - 8C12**
IRQ 4294967294	**Intel(R) 8 Series/C220 Series PCI Express Root Port #1 - 8C10**

Appendix D. BIOS Memory Map

Address	Device Description
0xFED40000-0xFED44FFF	System board
0xDF200000-0xFEAFFFFF	PCI Bus
0xA0000-0xBFFFF	PCI Bus
0xD0000-0xD3FFF	PCI Bus
0xD4000-0xD7FFF	PCI Bus
0xD8000-0xDBFFF	PCI Bus
0xDC000-0xDFFFF	PCI Bus
0xE0000-0xE3FFF	PCI Bus
0xE4000-0xE7FFF	PCI Bus
0xFED1C000-0xFED1FFFF	Motherboard resources
0xFED10000-0xFED17FFF	Motherboard resources
0xFED18000-0xFED18FFF	Motherboard resources
0xFED19000-0xFED19FFF	Motherboard resources
0xF8000000-0xFBFFFFFF	Motherboard resources
0xFED20000-0xFED3FFFF	Motherboard resources
0xFED90000-0xFED93FFF	Motherboard resources
0xFED45000-0xFED8FFFF	Motherboard resources
0xFF000000-0xFFFFFFFF	Motherboard resources
0xFEE00000-0xFEEFFFFF	Motherboard resources
0xF7FDF000-0xF7FDFFFF	Motherboard resources
0xF7FE0000-0xF7FEFFFF	Motherboard resources
0xF7D20000-0xF7D2FFFF	Intel(R) USB 3.0 Extensible Host Controller
0xF7D3F000-0xF7D3F00F	Intel(R) Management Engine Interface
0xF7C00000-0xF7CFFFFF	Intel(R) I210 Gigabit Network Connection
0xF7C80000-0xF7C83FFF	Intel(R) I210 Gigabit Network Connection
0xF7800000-0xF7BFFFFF	Intel(R) HD Graphics P4600/P4700
0xE0000000-0xEFFFFFFF	Intel(R) HD Graphics P4600/P4700
0xA0000-0xBFFFF	Intel(R) HD Graphics P4600/P4700
0xF7D00000-0xF7D1FFFF	Intel(R) Ethernet Connection I217-LM
0xF7D3D000-0xF7D3DFFF	Intel(R) Ethernet Connection I217-LM
0xFF000000-0xFFFFFFFF	Intel(R) 82802 Firmware Hub Device

Address	Device Description
0xF7D3C000-0xF7D3C3FF	Intel(R) 8 Series/C220 Series USB Enhanced Host Controller #2 - 8C2D
0xF7D3B000-0xF7D3B3FF	Intel(R) 8 Series/C220 Series USB Enhanced Host Controller #1 - 8C26
0xF7D39000-0xF7D390FF	Intel(R) 8 Series/C220 Series SMBus Controller - 8C22
0xF7D3A000-0xF7D3A7FF	Intel(R) 8 Series/C220 Series SATA AHCI Controller - 8C02
0xF7C00000-0xF7CFFFFF	Intel(R) 8 Series/C220 Series PCI Express Root Port #4 - 8C16
0xFED00000-0xFED003FF	High precision event timer
0xF7D30000-0xF7D33FFF	High Definition Audio Controller
0xF7D34000-0xF7D37FFF	High Definition Audio Controller

Appendix E. Direct Memory Access

Resource	Device
Channel 4	Direct memory access controller

Appendix F. Watchdog Timer (WDT) Setting

WDT is widely used for industrial application to monitor CPU activities. The application software depends on its requirement to trigger WDT with adequate timer setting. Before WDT timeout, the functional normal system will reload the WDT. The WDT never time-out for a normal system. The WDT will not be reloaded by an abnormal system, then WDT will time-out and auto-reset the system to avoid abnormal operation.

This computer supports 255 levels watchdog timer by software programming I/O ports.

Below is an program example to disable and load WDT.

Sample Codes:

```
/*-----   Include Header Area -----*/
#include "math.h"
#include "stdio.h"
#include "dos.h"

#define SIO_INDEX       0x2E            /* or index = 0x4E */
#define SIO_DATA        0x2F            /* or data  = 0x4F */

/*-----   routing, sub-routing -----*/
void main()
{
          outportb(sioIndex, 0x87);                     /* SIO - Enable */
          outportb(sioIndex, 0x87);

          outportb(sioIndex, 0x07);                     /* LDN - WDT */
          outportb(sioData,  0x07);

          outportb(sioIndex, 0x30);                     /* WDT - Enable */
          outportb(sioData,  0x01);

          outportb(sioIndex, 0xF0);                     /* WDOUT_EN */
          outportb(sioData,  0x80);

          outportb(sioIndex, 0xF6);                     /* WDT - Timeout Value */
          outportb(sioData,  0x05);

          outportb(sioIndex, 0xF5);                     /* WDT - Configuration */
          outportb(sioData,  0x72);

          outportb(sioIndex, 0xAA);                     /* SIO - Disable */
}
```

Appendix G. Digital I/O Setting

Digital I/O can read from or write to a line or an entire digital port, which is a collection of lines. This mechanism helps users achieve various applications such as industrial automation, customized circuit, and laboratory testing. Take the source code below that is written in C for the digital I/O application example.

Sample Codes:

```
/*-----   Include Header Area -----*/
#include "math.h"
#include "stdio.h"
#include "dos.h"

#define    DELAY_TIME                              10

int SMB_PORT_AD    = 0xF040;
int SMB_DEVICE_ADD = 0x9c;              /* Add = 6eh or 9ch */

unsigned char DIO_Set(unsigned char oMode, unsigned char oData);
unsigned char SMB_Byte_READ(int SMPORT, int DeviceID, int iREG_INDEX);
void SMB_Byte_WRITE(int SMPORT, int DeviceID, int oREG_INDEX, int oREG_DATA);

/*-----   routing, sub-routing -----*/
void main()
{
    unsigned char DataIn;

    Digital_Output(0x55);
    delay(2000);

    DataIn = Digital_Input();
    printf(" Input : %2x \n",DataIn);
    delay(2000);

    Digital_Output(0xAA);
    delay(2000);

    DataIn = Digital_Input();
    printf(" Input : %2x \n",DataIn);
    delay(2000);
}

unsigned char Digital_Input(void)
{
          unsigned char bData;

    /* DIO In 0~7 Mode */
          SMB_Byte_WRITE(SMB_PORT_AD,SMB_DEVICE_ADD,0x20,0x00);
    delay(DELAY_TIME);

          /* DIO In 0~7 Status */
          bData = SMB_Byte_READ(SMB_PORT_AD,SMB_DEVICE_ADD,0x22);

    return bData;
}

void Digital_Output(unsigned char oData)
{
          unsigned char bData;
```

```
    /* DIO Out 0~7 Mode */
          SMB_Byte_WRITE(SMB_PORT_AD,SMB_DEVICE_ADD,0x10,0xff);
    delay(DELAY_TIME);

    /* DIO Out 0~7 Data */
          SMB_Byte_WRITE(SMB_PORT_AD,SMB_DEVICE_ADD,0x11,oData);
    delay(DELAY_TIME);

    return bData;
}
```

Note: If any further support about SM bus is needed, please contact our FAE.

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